Cyclone V Device Handbook

Volume 1: Device Overview and Datasheet

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Contents

Additional Information

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The chapters in this document, Cyclone V Device Handbook, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1. Overview for Cyclone V Device Family
Revised: *November 2011*
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Chapter 2. Device Datasheet for Cyclone V Devices
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1. Overview for Cyclone V Device Family

CV-51001-1.1

Cyclone® V devices are designed to simultaneously accommodate the shrinking power consumption, cost, and time-to-market requirements; and the increasing bandwidth requirements for high-volume and cost-sensitive applications.

The Cyclone V devices are ideal for small form factor applications that are cost- and power-sensitive in the wireless, wireline, military, broadcast, industrial, consumer, and communications industries.

The Cyclone V device family is available in six variants:

- Cyclone V E—optimized for the lowest system cost and power requirement for a wide spectrum of general logic and digital signal processing (DSP) applications.
- Cyclone V GX—optimized for the lowest cost and power requirement for 614-megabits per second (Mbps) to 3.125-gigabits per second (Gbps) transceiver applications.
- Cyclone V GT—the FPGA industry's lowest cost and lowest power requirement for 5-Gbps transceiver applications.
- Cyclone V SE—system-on-a-chip (SoC) FPGA with integrated Cyclone V FPGA and ARM®-based hard processor system (HPS).
- Cyclone V SX—SoC FPGA with integrated Cyclone V FPGA, ARM-based HPS, and 3.125-Gbps transceivers.
- Cyclone V ST—SoC FPGA with integrated Cyclone V FPGA, ARM-based HPS, and 5-Gbps transceivers.

The Cyclone V SoC FPGA variants feature an FPGA integrated with an HPS that consists of a dual-core ARM Cortex™-A9 MPCore™ processor, a rich set of peripherals, and a shared multiport SDRAM controller.

The Cyclone V device family provides the following key advantages:

- Up to 40% lower power consumption than the previous generation device—built on TSMC's 28-nm low power (28LP) process and includes an abundance of hard intellectual properties (IP).
- Improved logic integration and differentiation capabilities—features a new 8-input adaptive logic module (ALM), up to 11.6 megabits (Mb) of dedicated memory, and variable-precision DSP blocks.
- Increased bandwidth capacity—a combined result of the new 3-Gbps and 5-Gbps transceivers, and the hard memory controllers.
- Tight integration of a dual-core ARM Cortex-A9 MPCore processor, hard IP, and an FPGA in a single Cyclone V SoC FPGA—supports over 100 Gbps peak bandwidth with integrated data coherency between the processor and the FPGA.

Cyclone V Features Summary

Some of the key features of the Cyclone V devices include:

- Built-in hard IP blocks
- Support for all mainstream single-ended and differential I/O standards including 3.3 V at up to 16 mA drive strengths
- HPS for the Cyclone V SE, SX, and ST variants
- Comprehensive design protection features to protect your valuable IP investments
- Lowest system cost advantage—requires only two core voltages to operate, are available in low-cost wirebond packaging, and includes innovative cost saving features such as Configuration via Protocol (CvP) and partial reconfiguration

Table 1–1 lists a summary of the Cyclone V features.

Table 1–1. Summary of Features for Cyclone V Devices (Part 1 of 2)

Feature	Details	
Technology	■ TSMC's 28-nm low power (28LP) process technology ■ 1.1-V core voltage	
Low-power high-speed serial interface	■ 614 Mbps to 5.0 Gbps integrated transceiver speed ■ Transmitter pre-emphasis and receiver equalization ■ Dynamic partial reconfiguration of individual channels	
FPGA General-purpose I/Os (GPIOs)	■ 875 Mbps LVDS receiver and 840 Mbps LVDS transmitter ■ 400 MHz/800 Mbps external memory interface ■ On-chip termination (OCT) ■ 3.3-V support with up to 16 mA drive strength	
Hard IP blocks	Embedded transceiver I/O	PCI Express® (PCIe®) Gen2 (x1 or x2) and Gen1 (x1, x2, or x4) hard IP with multifunction support, endpoint, and root port
	Variable-precision DSP	■ Native support for three signal processing precision levels (three 9 x 9s, two 18 x 19s, or one 27 x 27 multiplier) in the same variable-precision DSP block ■ 64-bit accumulator and cascade ■ Embedded internal coefficient memory ■ Preadder/subtractor for improved efficiency
	Memory controller	DDR3, DDR2, LPDDR, and LPDDR2

Table 1–1. Summary of Features for Cyclone V Devices (Part 2 of 2)

Feature	Details
HPS (Cyclone V SE, SX, and ST devices only)	■ Dual-core ARM Cortex-A9 MPCore processor—up to 800 MHz maximum frequency with support for symmetric and asymmetric multiprocessing ■ Interface peripherals—10/100/1000 Ethernet media access control (MAC), USB 2.0 On-The-GO (OTG) controller, serial peripheral interface (SPI), Quad SPI flash controller, NAND flash controller, SD/MMC/SDIO controller, UART, controller area network (CAN), I2C interface, and up to 71 HPS I/O interfaces ■ System peripherals—general-purpose and watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managers ■ On-chip RAM and boot ROM ■ HPS–FPGA bridges—include the FPGA-to-HPS, HPS-to-FPGA, and lightweight HPS-to-FPGA bridges that allow the FPGA fabric to master transactions to slaves in the HPS, and vice versa. ■ FPGA-to-HPS SDRAM controller subsystem—provides a configurable interface to the multiport front end (MPFE) of the HPS SDRAM controller ■ ARM CoreSight™ JTAG debug access port, trace port, and on-chip trace storage
High-performance FPGA fabric	Enhanced 8-input ALM with four registers
Internal memory blocks	■ M10K—10-kilobits (Kb) memory blocks with soft error correction code (ECC) ■ Memory logic array block (MLAB)—640-bit distributed LUTRAM where you can use up to 25% of the ALMs as MLAB memory
Phase-locked loops (PLLs)	■ Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB) ■ Integer mode and fractional mode
Clock networks	■ 550 MHz global clock network ■ Global, quadrant, and peripheral clock networks ■ Clock networks that are not used can be powered down to reduce dynamic power
Configuration	■ Partial and dynamic reconfiguration of the FPGA ■ CvP ■ Active serial (AS) x1 and x4, fast passive parallel (FPP) x8 and x16, passive serial (PS), and JTAG options ■ Enhanced advanced encryption standard (AES) design security features ■ Tamper protection
Packaging	■ Wirebond low-halogen packages ■ Multiple device densities with compatible package footprints for seamless migration between different device densities ■ RoHS-compliant options

Cyclone V Family Plan

Table 1–2 and Table 1–3 list the Cyclone V E, GX, and GT maximum resource counts.

Table 1–2. Maximum Resource Counts for Cyclone V E Devices—*Preliminary*

Resource	Cyclone V E Device				
	5CEA2	5CEA4	5CEA5	5CEA7	5CEA9
ALM	9,434	18,113	28,868	56,415	113,585
Logic Element (LE)	25,000	48,000	76,500	149,500	301,000
Block Memory (Kb)	1,700	2,700	3,800	6,500	11,600
MLAB Memory (Kb)	196	270	440	836	1,717
Variable-precision DSP Block	25	72	124	156	342
18 x 19 Multiplier	50	144	248	312	684
Fractional PLL	4	4	6	6	6
GPIO	304	304	360	488	488
LVDS	100	100	100	122	122
Hard Memory Controller	1	1	2	2	2

Table 1–3. Maximum Resource Counts for Cyclone V GX and GT Devices—*Preliminary*

Resource	Cyclone V GX Device					Cyclone V GT Device		
	5CGXC3	5CGXC4	5CGXC5	5CGXC7	5CGXC9	5CGTD5	5CGTD7	5CGTD9
ALM	11,698	18,868	28,868	56,415	113,585	28,868	56,415	113,585
LE	31,000	50,000	76,500	149,500	301,000	76,500	149,500	301,000
Block Memory (Kb)	1,400	2,500	3,800	6,500	11,600	3,800	6,500	11,600
MLAB Memory (Kb)	188	295	440	836	1,717	440	836	1,717
Variable-precision DSP Block	42	70	124	156	342	124	156	342
18 x 19 Multiplier	84	140	248	312	684	248	312	684
Fractional PLL (1)	4	6	6	7	8	6	7	8
3-Gbps Transceiver	3	6	6	9	12	—	—	—
5-Gbps Transceiver	—	—	—	—	—	6	9	12
GPIO	224	368	368	480	560	368	480	560
LVDS	48	90	100	122	122	100	122	122
PCIe Hard IP Block	1	2	2	2	2	2	2	2
Hard Memory Controller	1	2	2	2	2	2	2	2

Note to Table 1–3:

(1) The maximum fractional PLLs listed include general purpose PLLs and transceiver PLLs.

Table 1–4 and Table 1–5 list the Cyclone V SE, SX, and ST maximum resource counts.

Table 1–4. Maximum Resource Counts for Cyclone V SE Devices—*Preliminary*

Resource	Cyclone V SE Devices			
	5CSEA2	5CSEA4	5CSEA5	5CSEA6
ALM	9,434	15,094	32,075	41,509
LE	25,000	40,000	85,000	110,000
Block Memory (Kb)	1,400	2,240	3,972	5,140
MLAB Memory (Kb)	138	220	480	621
Variable-precision DSP Block	36	58	87	112
18 x 19 Multiplier	72	116	174	224
FPGA Fractional PLL	4	5	6	6
HPS PLL	3	3	3	3
FPGA GPIO	124	124	288	288
HPS I/O	188	188	188	188
LVDS	31	31	72	72
FPGA Memory Controller	—	1	1	1
HPS Memory Controller	1	1	1	1
ARM Cortex-A9 MPCore Processor	Single- or dual-core	Single- or dual-core	Single- or dual-core	Single- or dual-core

Table 1–5. Maximum Resource Counts for Cyclone V SX and ST Devices—*Preliminary*

Resource	Cyclone V SX Device			Cyclone V ST Device	
	5CSXC4	5CSXC5	5CSXC6	5CSTD5	5CSTD6
ALM	15,094	32,075	41,509	32,075	41,509
LE	40,000	85,000	110,000	85,000	110,000
Block Memory (Kb)	2,240	3,972	5,140	3,972	5,140
MLAB Memory (Kb)	220	480	621	480	621
Variable-precision DSP Block	58	87	112	87	112
18 x 19 Multiplier	116	174	224	174	224
FPGA Fractional PLL (1)	5	6	6	6	6
HPS PLL	3	3	3	3	3
3-Gbps Transceiver	6	9	9	—	—
5-Gbps Transceiver	—	—	—	9	9
FPGA GPIO	124	288	288	288	288
HPS I/O	188	188	188	188	188
LVDS	31	72	72	72	72
PCIe Hard IP Block	2	2	2	2	2
FPGA Memory Controller	1	1	1	1	1
HPS Memory Controller	1	1	1	1	1
ARM Cortex-A9 MPCore Processor	Dual-core	Dual-core	Dual-core	Dual-core	Dual-core

Note to Table 1–5:

(1) The maximum FPGA fractional PLLs listed include FPGA general purpose PLLs and transceiver PLLs.

Table 1–6 lists the Cyclone V E, GX, and GT package plan that shows the GPIO count, the maximum number of transceivers available, and the vertical migration capability for each device package and density.

Table 1–6. Package Plan for Cyclone V E, GX, and GT Devices—*Preliminary* (1)

Device	F256 (17 mm)		U324 (15 mm)		U484 (19 mm)		F484 (23 mm)		F672 (27 mm)		F896 (31 mm)		F1152 (35 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
5CEA2	144	—	TBD	—	304	—	304	—	—	—	—	—	—	—
5CEA4	144	—	TBD	—	304	—	304	—	—	—	—	—	—	—
5CEA5	—	—	—	—	238	—	240	—	360	—	—	—	—	—
5CEA7	—	—	—	—	230	—	240	—	336	—	488	—	—	—
5CEA9	—	—	—	—	—	—	230	—	336	—	488	—	—	—
5CGXC3 (2)	97	3	112	3	224	3	224	3	—	—	—	—	—	—
5CGXC4 (2)	—	—	—	—	240	6	240	6	368	6	—	—	—	—
5CGXC5 (2)	—	—	—	—	240	6	240	6	368	6	—	—	—	—
5CGTD5 (3)	—	—	—	—	240	6	240	6	368	6	—	—	—	—
5CGXC7 (2)	—	—	—	—	240	6	240	6	336	9	480	9	—	—
5CGTD7 (3)	—	—	—	—	240	6	240	6	336	9	480	9	—	—
5CGXC9 (2)	—	—	—	—	—	—	230	6	336	9	448	12	560	12
5CGTD9 (3)	—	—	—	—	—	—	230	6	336	9	448	12	560	12

Notes to Table 1–6:

(1) The arrows indicate the package vertical migration capability. You can also migrate your design across device densities in the same packaging option if the devices have the same dedicated pins, configuration pins, and power pins.

(2) The transceiver counts listed are for 3-Gbps transceivers.

(3) The transceiver counts listed are for 5-Gbps transceivers.

Table 1–7 lists the Cyclone V SE, SX, and ST package plan that shows the FPGA GPIO and HPS I/O counts, the maximum number of transceivers available, and the vertical migration capability for each device package and density.

Table 1–7. Package Plan for Cyclone V SE, SX, and ST Devices—*Preliminary* *(1)*

Device	U484 (19 mm)			U672 (23 mm)			F896 (31 mm)		
	GPIO	XCVR	HPS I/O	GPIO	XCVR	HPS I/O	GPIO	XCVR	HPS I/O
5CSEA2	66	—	161	124	—	188	—	—	—
5CSEA4	66	—	161	124	—	188	—	—	—
5CSEA5	66	—	161	124	—	188	288	—	188
5CSEA6	66	—	161	124	—	188	288	—	188
5CSXC4 *(2)*	—	—	—	124	6	188	—	—	—
5CSXC5 *(2)*	—	—	—	124	6	188	288	9	188
5CSXC6 *(2)*	—	—	—	124	6	188	288	9	188
5CSTD5 *(3)*	—	—	—	—	—	—	288	9	188
5CSTD6 *(3)*	—	—	—	—	—	—	288	9	188

Notes to Table 1–7:

(1) The arrows indicate the package vertical migration capability. You can also migrate your design across device densities in the same packaging option if the devices have the same dedicated pins, configuration pins, and power pins.

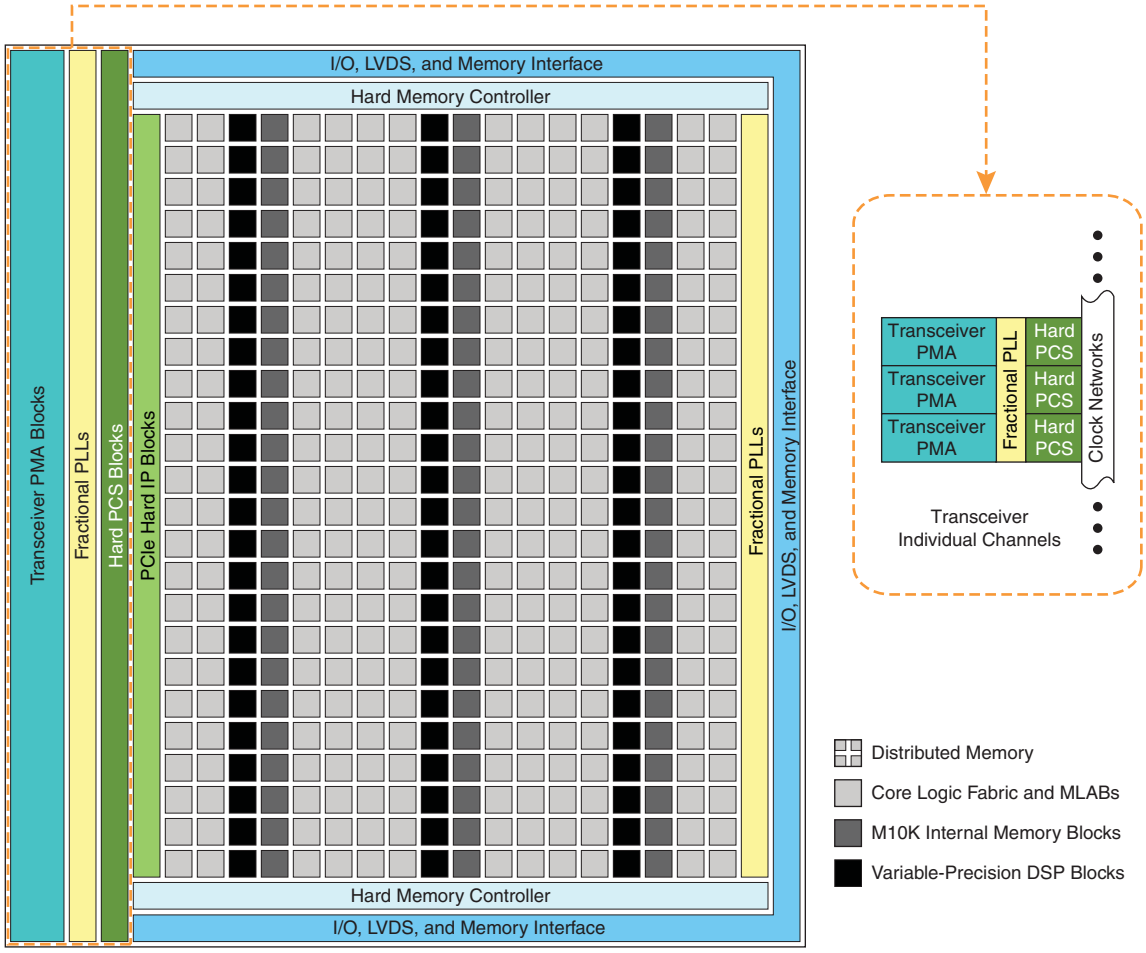
(2) The transceiver counts listed are for 3-Gbps transceivers.

(3) The transceiver counts listed are for 5-Gbps transceivers.

Low-Power Serial Transceivers

Cyclone V devices deliver the industry's lowest power 5-Gbps transceivers at an estimated 88 mW maximum power consumption per channel. Cyclone V transceivers are designed to be compliant for a wide range of protocols and data rates. The transceivers are positioned on the left outer edge of the device, as shown in Figure 1–1. The transceiver channels consist of the physical medium attachment (PMA), physical coding sublayer (PCS), and clock networks.

Figure 1–1. Device Chip Overview for Cyclone V Devices *(1)*



Note to Figure 1–1:

(1) This figure represents a Cyclone V device with transceivers. Other Cyclone V devices may have a different floor plan than the one shown here.

PMA Support

To prevent core and I/O noise from coupling into the transceivers, the PMA block is isolated from the rest of the chip—ensuring optimal signal integrity. For the transceivers, you can use the channel PLL of an unused receiver PMA as an additional transmit PLL.

Table 1–8 lists the PMA features of the transceiver.

Table 1–8. PMA Features of the Transceivers in Cyclone V Devices

Features	Capability
Backplane support	Up to 16” FR4 PCB fabric drive capability at up to 5 Gbps
PLL-based clock recovery	Superior jitter tolerance
Programmable deserialization and word alignment	Flexible deserialization width and configurable word alignment pattern
Equalization and pre-emphasis	Up to 6 dB of pre-emphasis, up to 4 dB of equalization, and no decision feedback equalizer (DFE)
Ring oscillator transmit PLLs	614 Mbps to 5 Gbps
Input reference clock range	20 MHz to 400 MHz
Transceiver dynamic reconfiguration	Allows the reconfiguration of a single channel without affecting the operation of other channels

PCS Support

The Cyclone V core logic connects to the PCS through an 8-, 10-, 16-, 20-, 32-, or 40-bit interface, depending on the transceiver data rate and protocol. Cyclone V devices contain PCS hard IP to support PCIe Gen1 and Gen2, XAUI, Gbps Ethernet (GbE), Serial RapidIO® (SRIO), and Common Public Radio Interface (CPRI). Most of the other standard and proprietary protocols from 614 Mbps to 5.0 Gbps are supported.

Table 1–9 lists the PCS features of the transceiver.

Table 1–9. PCS Features of the Transceivers in Cyclone V Devices (Part 1 of 2)

PCS Support	Data Rates (Gbps)	Transmitter Datapath	Receiver Datapath
3-Gbps and 5-Gbps Basic	0.614 to 5.0	■ Phase compensation FIFO ■ Byte serializer ■ 8B/10B encoder ■ Transmitter bit-slip	■ Word aligner ■ Deskew FIFO ■ Rate-match FIFO ■ 8B/10B decoder ■ Byte deserializer ■ Byte ordering ■ Receiver phase compensation FIFO
PCIe Gen1: x1, x2, x4 PCIe Gen2: x1, x2 *(1)*	2.5 and 5.0	■ Dedicated PCIe PHY IP core ■ PIPE 2.0 interface to the core logic	■ Dedicated PCIe PHY IP core ■ PIPE 2.0 interface to the core logic
GbE	1.25	■ Custom PHY IP core with preset feature ■ GbE transmitter synchronization state machine	■ Custom PHY IP core with preset feature ■ GbE receiver synchronization state machine

Table 1–9. PCS Features of the Transceivers in Cyclone V Devices (Part 2 of 2)

PCS Support	Data Rates (Gbps)	Transmitter Datapath	Receiver Datapath
XAUI	3.125	■ Dedicated XAUI PHY IP core ■ XAUI synchronization state machine for bonding four channels	■ Dedicated XAUI PHY IP core ■ XAUI synchronization state machine for realigning four channels
SRIO 1.3 and 2.1	1.25 to 3.125	■ Custom PHY IP core with preset feature ■ SRIO version 2.1-compliant x2 and x4 channel bonding	■ Custom PHY IP core with preset feature ■ SRIO version 2.1-compliant x2 and x4 deskew state machine
SDI, SD/HD, and 3G-SDI	0.27 (2), 1.485, and 2.97	■ Custom PHY IP core with preset feature	■ Custom PHY IP core with preset feature
Serial ATA Gen1 and Gen2	1.5 and 3.0	■ Custom PHY IP core with preset feature ■ Electrical idle	■ Custom PHY IP core with preset feature ■ Signal detect ■ Wider spread of asynchronous SSC
CPRI 4.1 (3)	0.6144 to 4.9152	■ Dedicated deterministic latency PHY IP core ■ Transmitter (TX) manual bit-slip mode	■ Dedicated deterministic latency PHY IP core ■ Receiver (RX) deterministic latency state machine
OBSAI RP3	0.768 to 3.072	■ Dedicated deterministic latency PHY IP core ■ TX manual bit-slip mode	■ Dedicated deterministic latency PHY IP core ■ RX deterministic latency state machine
V-by-One HS	Up to 3.75	Custom PHY IP core	■ Custom PHY IP core ■ Wider spread of asynchronous SSC
DisplayPort 1.2 (4)	1.62 and 2.7	Custom PHY IP core	■ Custom PHY IP core ■ Wider spread of asynchronous SSC
HiGig	3.75	■ Dedicated XAUI PHY IP core ■ XAUI synchronization state machine for bonding four channels	■ Dedicated XAUI PHY IP core ■ XAUI synchronization state machine for realigning four channels
JESD204A	0.3125 (2) to 3.125	Custom PHY IP core with preset feature	Custom PHY IP core with preset feature

Notes to Table 1–9:

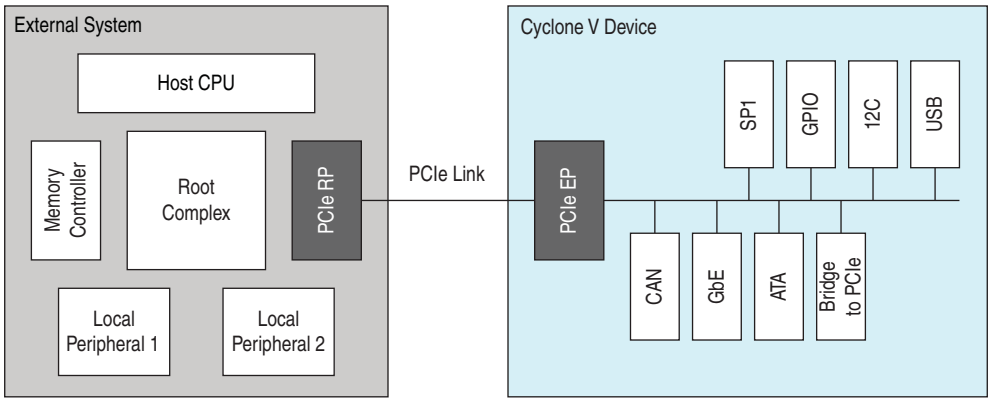
(1) PCIe Gen2 is supported only for Cyclone V GT devices.
(2) The 0.27-Gbps and 0.3125-Gbps data rates are supported using oversampling user logic that you must implement in the FPGA fabric.
(3) High-voltage output mode (1000-BASE-CX) is not supported.
(4) Pending characterization.

PCIe Gen1 and Gen2 Hard IP

Cyclone V GX, GT, SX, and ST devices contain PCIe hard IP—consisting of the MAC, data link, and transaction layers—that is designed for performance, ease-of-use, and increased functionality. The PCIe hard IP supports PCIe Gen2 end point and root port for x1 and x2 lanes configuration, and Gen1 end point and root port for up to x4 lane configuration.

The PCIe endpoint support includes multifunction support for up to eight functions, as shown in Figure 1–2. The integrated multifunction support reduces the FPGA logic requirements by up to 20 K LEs for PCIe designs that require multiple peripherals.

Figure 1–2. PCIe Multifunction for Cyclone V Devices



The Cyclone V PCIe hard IP operates independently from the core logic. This independent operation allows the PCIe link to wake up and complete link training in less than 100 ms while the Cyclone V device completes loading the programming file for the rest of the device. In addition, the PCIe hard IP in the Cyclone V device provides improved end-to-end datapath protection using ECC.

FPGA GPIOs

Cyclone V devices offer highly configurable GPIOs. The following list describes the many features of the GPIOs:

- Programmable bus hold and weak pull-up.
- **LVDS** output buffer with programmable differential output voltage (V_{OD}) and programmable pre-emphasis.
- Dynamic on-chip parallel termination (R_T OCT) for all I/O banks with OCT calibration to limit the termination impedance variation to ±15%.
- On-chip dynamic termination that has the ability to swap between serial and parallel termination, depending on whether there is read or write on a common bus for signal integrity.
- Unused voltage reference (VREF) pins that can be configured as user I/Os.
- Easy timing closure support using the hard read FIFO in the input register path, and delay-locked loop (DLL) delay chain with fine and coarse architecture.

External Memory

Cyclone V devices support up to two hard memory controllers for DDR3, DDR2, LPDDR2, and LPDDR SDRAM devices. Each controller supports 8- to 32-bit components of up to 4 gigabits (Gb) in density with two chip selects and optional ECC. Cyclone V devices also support soft memory controllers for DDR3, DDR2, LPDDR2, and LPDDR SDRAM for maximum flexibility.

Table 1–10 lists the performance of the external memory interface in Cyclone V devices.

Table 1–10. External Memory Interface Performance in Cyclone V Devices

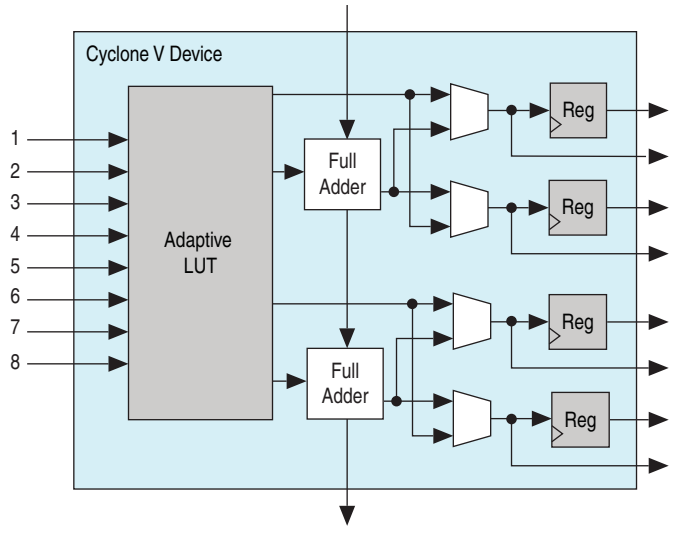
Interface	Voltage (V)	Hard Controller (MHz)	Soft Controller (MHz)
DDR3 SDRAM	1.5	400	300
DDR3L SDRAM	1.35	400	300
DDR3U SDRAM	1.25	333	300
DDR2 SDRAM	1.8	400	300
	1.5	400	300
LPDDR2 SDRAM	1.2	333	300
LPDDR SDRAM	1.8	200	200

Adaptive Logic Module

Cyclone V devices use a 28-nm ALM as the basic building block of the logic fabric. The ALM, as shown in Figure 1–3, uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than previous generations.

You can configure up to 25% of the ALMs in Cyclone V devices as distributed memory using MLABs. For more information, refer to "Embedded Memory" on page 1–15.

Figure 1–3. ALM for Cyclone V Devices



Variable-Precision DSP Block

Cyclone V devices feature a variable-precision DSP block that you can configure to support signal processing with precisions ranging from 9 x 9, 18 x 19, and 27 x 27 bits natively.

You can configure each DSP block during compilation as independent three 9 x 9, two 18 x 19, or one 27 x 27 multipliers. With a dedicated 64-bit cascade bus, you can cascade multiple variable-precision DSP blocks to implement even higher precision DSP functions efficiently.

The variable-precision DSP block also supports these features:

- A 64-bit accumulator that is the largest in the industry.
- A hard preadder that is available in both 18- and 27-bit modes.
- Cascaded output adders for efficient systolic finite impulse response (FIR) filters.
- Internal coefficient register banks, 8 deep, for each multiplier in 18- or 27-bit mode.
- Fully independent multiplier operation.
- A second accumulator feedback register to accommodate complex multiply-accumulate functions.
- Efficient support for single- and double-precision floating point arithmetic.
- The inferability of all modes by the Quartus® II design software.

Table 1–11 lists the relevant DSP block configurations for a few usage examples.

Table 1–11. Variable-Precision DSP Block Configurations for Cyclone V Devices

Usage	Multiplier Size (Bit)	DSP Block Resource
Low precision fixed point for video applications	Three 9 x 9	1 variable-precision DSP block
Medium precision fixed point in FIR filters	Two 18 x 19	1 variable-precision DSP block
FIR filters and general DSP usage	Two 18 x 19 with accumulate	1 variable-precision DSP block
High precision fixed- or floating-point implementations	One 27 x 27 with accumulate	1 variable-precision DSP block

Table 1–12 lists the variable-precision DSP resources by bit precision for each Cyclone V device.

Table 1–12. Number of Multipliers in Cyclone V Devices (Part 1 of 2)

Variant	Device	Variable-precision DSP Block	Independent Input and Output Multiplications Operator			18 x 19 Multiplier Adder Mode	18 x 18 Multiplier Adder Summed with 36-bit Input
			9 x 9 Multiplier	18 x 19 Multiplier	27 x 27 Multiplier		
Cyclone V E	5CEA2	25	75	50	25	25	25
	5CEA4	72	216	144	72	72	72
	5CEA5	124	372	248	124	124	124
	5CEA7	156	468	312	156	156	156
	5CEA9	342	1,026	684	342	342	342

Table 1–12. Number of Multipliers in Cyclone V Devices (Part 2 of 2)

Variant	Device	Variable-precision DSP Block	Independent Input and Output Multiplications Operator			18 x 19 Multiplier Adder Mode	18 x 18 Multiplier Adder Summed with 36-bit Input
			9 x 9 Multiplier	18 x 19 Multiplier	27 x 27 Multiplier		
Cyclone V GX	5CGXC3	42	126	84	42	42	42
	5CGXC4	70	210	140	70	70	70
	5CGXC5	124	372	248	124	124	124
	5CGXC7	156	468	312	156	156	156
	5CGXC9	342	1,026	684	342	342	342
Cyclone V GT	5CGTD5	124	372	248	124	124	124
	5CGTD7	156	468	312	156	156	156
	5CGTD9	342	1,026	684	342	342	342
Cyclone V SE	5CSEA2	36	108	73	36	36	36
	5CSEA4	58	174	116	58	58	58
	5CSEA5	87	261	173	87	87	87
	5CSEA6	112	336	224	112	112	112
Cyclone V SX	5CSXC4	36	108	73	36	36	36
	5CSXC5	58	174	116	58	58	58
	5CSXC6	87	261	173	87	87	87
Cyclone V ST	5CSTD5	87	261	173	87	87	87
	5CSTD6	112	336	224	112	112	112

Embedded Memory

The Cyclone V embedded memory blocks are flexible and designed to provide an optimal amount of small- and large-sized memory arrays. Cyclone V devices contain two types of embedded memory blocks:

- 640-bit MLAB blocks—ideal for wide and shallow memory arrays. The MLAB operates at up to 300 MHz.
- 10-Kb M10K blocks—ideal for larger memory arrays while still providing a large number of independent ports. The M10K embedded memory operates at up to 380 MHz.

Table 1–13 lists the supported memory configurations for Cyclone V devices.

Table 1–13. Embedded Memory Block Configurations for Cyclone V Devices

Memory Block	Depth (bits)	Programmable Widths
MLAB	32	x1, x2, x4, x8, x9, x10, x16, x18, or x20
M10K	256	x40 or x32
	512	x20 or x16
	1K	x10 or x8
	2K	x5 or x4
	4K	x2
	8K	x1

Dynamic and Partial Reconfiguration

The dynamic reconfiguration feature allows you to dynamically change the transceiver data rates, PMA settings, or protocols of a channel, without affecting data transfer on adjacent channels. This feature is ideal for applications that require on-the-fly multiprotocol or multirate support. You can reconfigure the PMA and PCS blocks with dynamic reconfiguration.

Partial reconfiguration allows you to reconfigure part of the device while other sections of the device remain operational. This capability is important in systems with critical uptime requirements because it allows you to make updates or adjust functionality without disrupting services.

Apart from lowering cost and power consumption, partial reconfiguration increases the effective logic density of the device because placing device functions that do not operate simultaneously is not necessary. Instead, you can store these functions in external memory and load them whenever the functions are required. This capability reduces the size of the device because it allows multiple applications on a single device—saving the board space and reducing the power consumption.

Altera simplifies the time-intensive task of partial reconfiguration by building this capability on top of the proven incremental compile and design flow in the Quartus II design software. With the Altera® solution, you do not need to know all the intricate device architecture details to perform a partial reconfiguration.

Partial reconfiguration is supported through the FPP x16 configuration interface. You can seamlessly use partial reconfiguration in tandem with dynamic reconfiguration to enable simultaneous partial reconfiguration of both the device core and transceivers.

Clock Networks and PLL Clock Sources

The Cyclone V clock network architecture is based on Altera's proven global, quadrant, and peripheral clock structure, which is supported by dedicated clock input pins and fractional PLLs. Cyclone V devices have 16 global clock networks capable of up to 550 MHz operation. The Quartus II software identifies all unused sections of the clock network and powers them down, which reduces power consumption.

Cyclone V devices have up to eight PLLs, each with nine output counters that you can use to reduce PLL usage in two ways:

- Reduce the number of oscillators that are required on your board by using fractional PLLs.
- Reduce the number of clock pins that are used in the device by synthesizing multiple clock frequencies from a single reference clock source.

Cyclone V devices use a fractional PLL architecture in addition to the historical integer PLL. If you use the fractional PLL mode, you can use the PLLs for precision fractional-N frequency synthesis—removing the need for off-chip reference clock sources in your design. The transceiver fractional PLLs that are not used by the transceiver I/Os can be used as general purpose fractional PLLs by the FPGA fabric.

Apart from frequency synthesis, on-chip clock deskew, jitter attenuation, counter reconfiguration, programmable output clock duty cycles, PLL cascading, and reference clock switchover, the PLLs in the Cyclone V devices also support the following key features:

- Programmable bandwidth
- User-mode reconfiguration of PLLs
- Reference clock switchover
- Dynamic phase shift
- Direct, source synchronous, ZDB, external feedback, and LVDS compensation

Enhanced Configuration and Configuration via Protocol

Cyclone V devices support 3.3-V programming voltage and several configuration modes. Table 1–14 lists the configuration modes and features supported by the Cyclone V devices.

Table 1–14. Configuration Modes and Features for Cyclone V Devices

Mode	Data Width (Bit)	Maximum Clock Rate (MHz)	Maximum Data Rate (Mbps)	Decompression	Design Security	Remote System Update	Partial Reconfiguration
AS through the EPCS and EPCQ serial configuration device	x1, x4	80	—	✓	✓	✓	—
PS through CPLD or external microcontroller	x1	125	125	✓	✓	—	—
FPP	x8, x16	125	—	✓	✓	Parallel flash loader	16-bit only
CvP (PCIe)	x1, x2, x4 (1)	—	—	—	✓	✓	✓
JTAG	x1	33	33	—	—	—	

Note to Table 1–14:

(1) The number of lanes instead of bit.

Instead of using an external flash or ROM, you can configure the Cyclone V devices through PCIe using CvP. The CvP mode offers the fastest configuration rate and flexibility with the easy-to-use PCIe hard IP block interface. The Cyclone V CvP implementation conforms to the PCIe 100 ms power-up-to-active time requirement.

Power Management

Leveraging the FPGA architectural features, process technology advancements, and transceivers that are designed for power efficiency, the Cyclone V devices consume less power than previous generation Cyclone FPGAs:

- Total device core power consumption—less by up to 40%.
- Transceiver channel power consumption—less by up to 50%.

Additionally, Cyclone V devices contain several hard IP blocks that reduce logic resources and deliver substantial power savings of up to 25% less power than equivalent soft implementations.

SoC FPGA with HPS

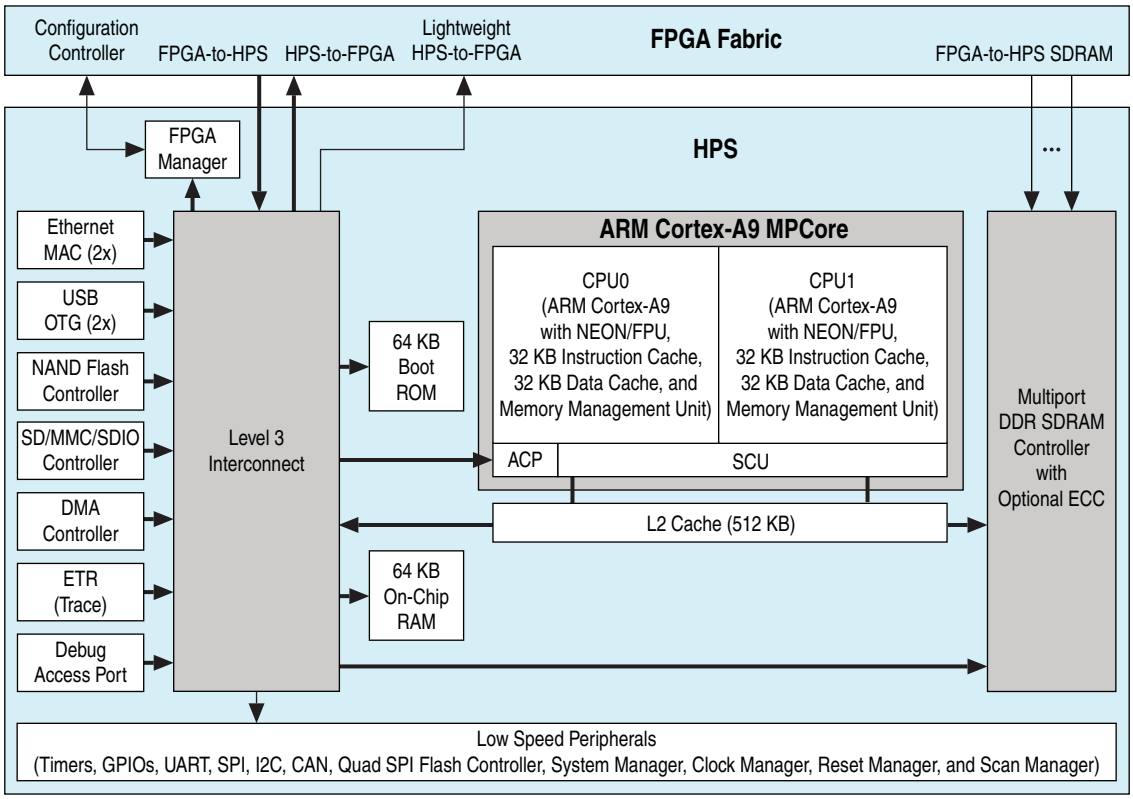
Each SoC FPGA combines an FPGA fabric and an HPS in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in these ways:

- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor
- Allows you to differentiate the end product in both hardware and software, and to support virtually any interface standard
- Extends the product life and revenue through in-field hardware and software updates

Features of the HPS

The HPS consists of a dual-core ARM Cortex-A9 MPCore processor, a rich set of peripherals, and a shared multiport SDRAM memory controller, as shown in Figure 1–4.

Figure 1–4. HPS with Dual-Core ARM Cortex-A9 MPCore Processor



System Peripherals

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC/SDIO controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. The debug access port provides interfaces to industry standard JTAG debug probes and supports ARM CoreSight debug and core traces to facilitate software development.

HPS–FPGA AXI Bridges

The HPS–FPGA bridges, which support the Advanced Microcontroller Bus Architecture (AMBA®) Advanced eXtensible Interface (AXI™) specifications, consist of the following bridges:

- FPGA-to-HPS AXI bridge—a high-performance bus supporting 32-, 64-, and 128-bit data widths that allows the FPGA fabric to master transactions to the slaves in the HPS
- HPS-to-FPGA AXI bridge—a high-performance bus supporting 32-, 64-, and 128-bit data widths that allows the HPS to master transactions to the slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA AXI bridge—a lower performance 32-bit width bus that allows the HPS to master transactions to the slaves in the FPGA fabric.

The HPS–FPGA AXI bridges also allow the FPGA fabric to access the memory shared by one or both microprocessors, and provide asynchronous clock crossing with the clock from the FPGA fabric.

HPS SDRAM Controller Subsystem

The HPS SDRAM controller subsystem contains a multiport SDRAM memory controller and DDR PHY that are shared between the FPGA fabric (through the FPGA-to-HPS SDRAM interface), the level 2 (L2) cache, and the level 3 (L3) system interconnect. The FPGA-to-HPS SDRAM interface supports AMBA AXI and Avalon® Memory-Mapped (Avalon-MM) interface standards, and provides up to four ports with separate read and write directions.

To maximize memory performance, the SDRAM controller subsystem supports command and data reordering, deficit round-robin arbitration with aging, and high-priority bypass features. The SDRAM controller subsytem supports DDR2, DDR3, LPDDR, or LPDDR2 devices up to 4 Gb in density and runs up to 400 MHz (800 Mbps data rate).

For easy migration, the FPGA-to-HPS SDRAM interface is compatible with the interface of the soft SDRAM memory controller IPs and hard SDRAM memory controllers in the FPGA fabric.

FPGA Configuration and Processor Booting

The FPGA fabric and HPS in the SoC FPGA are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power, or shut down the entire FPGA fabric to reduce total system power.

You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility:

- You can boot the HPS before you power up and configure the FPGA fabric. After the system is running, the HPS reconfigures the FPGA fabric at any time under program control or through the FPGA configuration controller.
- You can power up both the HPS and the FPGA fabric together, configure the FPGA fabric first, and then upload the boot code to the HPS from the FPGA fabric.

Hardware and Software Development

For hardware development, you can configure the HPS and connect your soft logic in the FPGA fabric to the HPS interfaces using the Qsys system integration tool in the Quartus II software.

For software development, the ARM-based SoC FPGA devices inherit the rich software development ecosystem available for the ARM Cortex-A9 MPCore processor. The software development process for Altera SoC FPGAs follows the same steps as those for other SoC devices. Altera also provides support for the Linux and VxWorks® operating systems.

You can begin device-specific firmware and software development on the Altera SoC FPGA Virtual Target. The Virtual Target is a fast PC-based functional simulation of a target development system—a model of a complete development board that runs on a PC. The Virtual Target enables the development of device-specific production software that can run unmodified on actual hardware.

Ordering Information

Figure 1–5 and Figure 1–6 show sample ordering codes and list the options available for Cyclone V E, GX, and GT devices.

Figure 1–5. Ordering Information for Cyclone V E Devices—*Preliminary*

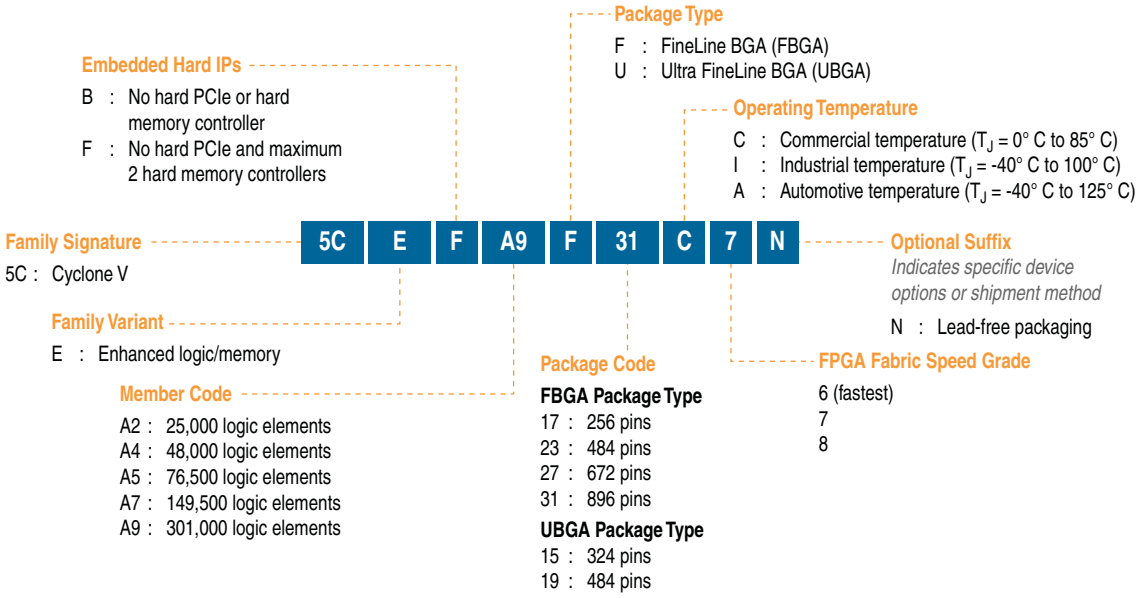


Figure 1–6. Ordering Information for Cyclone V GX and GT Devices—*Preliminary*

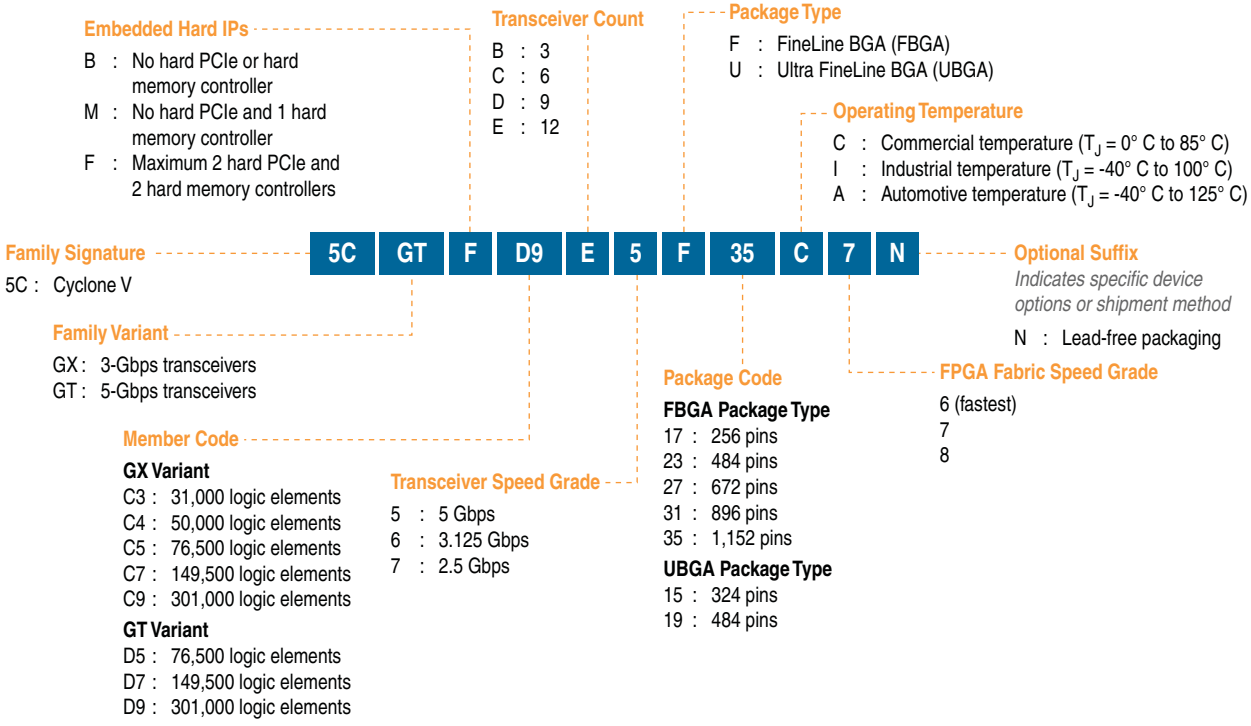


Figure 1–7 and Figure 1–8 show sample ordering codes and list the options available for Cyclone V SE, SX, and ST Devices.

Figure 1–7. Ordering Information for Cyclone V SE Devices—*Preliminary*

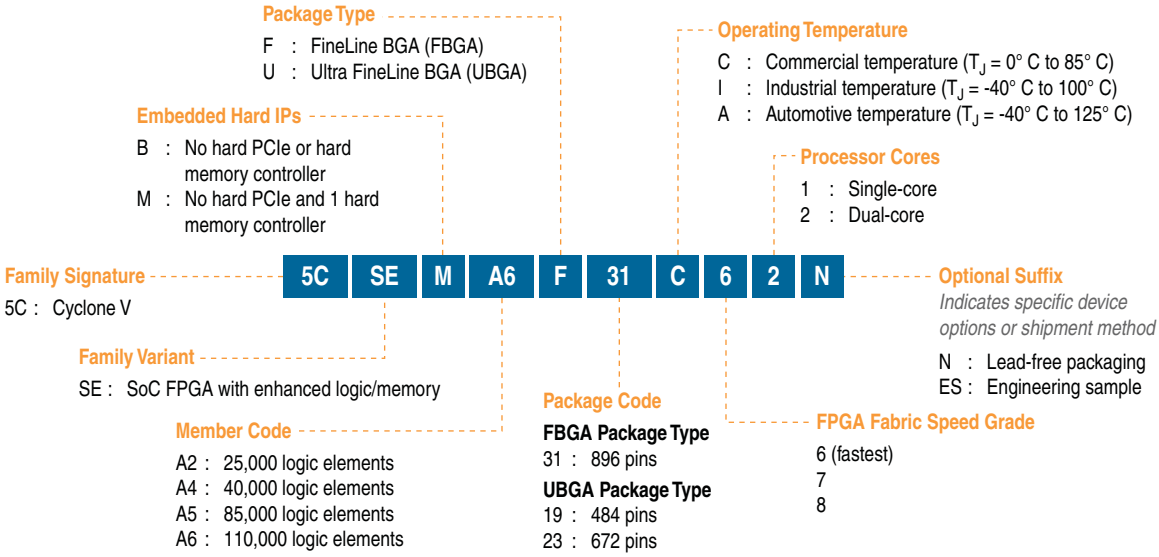
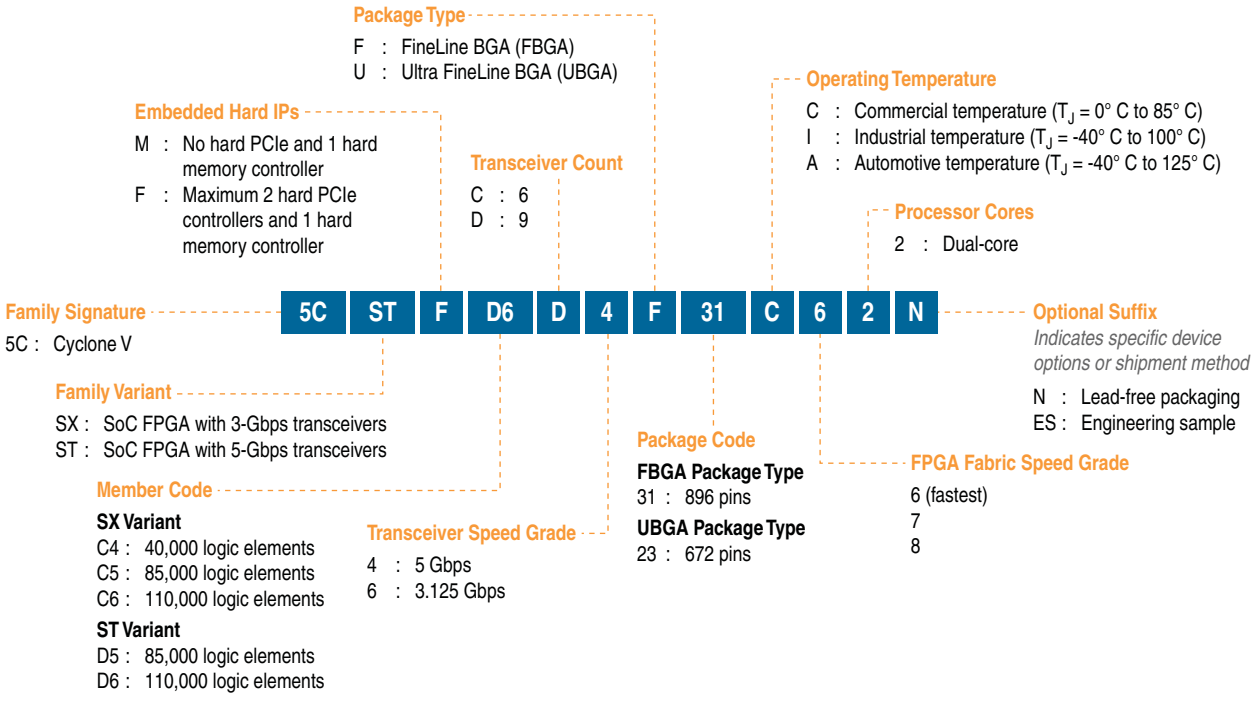


Figure 1–8. Ordering Information for Cyclone V SX and ST Devices—*Preliminary*



Document Revision History

Table 1–15 lists the revision history for this document.

Table 1–15. Document Revision History

Date	Version	Changes
November 2011	1.1	■ Updated Table 1–1, Table 1–2, Table 1–3, Table 1–4, Table 1–5, and Table 1–6. ■ Updated Figure 1–4, Figure 1–5, Figure 1–6, Figure 1–7, and Figure 1–8. ■ Updated "System Peripherals" on page 1–19, "HPS–FPGA AXI Bridges" on page 1–20, "HPS SDRAM Controller Subsystem" on page 1–20, "FPGA Configuration and Processor Booting" on page 1–20, and "Hardware and Software Development" on page 1–21. ■ Minor text edits.
October 2011	1.0	Initial release.

2. Device Datasheet for Cyclone V Devices

CV-51002-1.1

This chapter describes the electrical characteristics, switching characteristics, and configuration specifications for Cyclone® V devices. Electrical characteristics include operating conditions and power consumption. Switching characteristics list the transceiver specifications, and core and periphery performance. Configuration specifications cover power-on reset (POR) specifications, various configuration mode timing parameters, remote system upgrades timing, and user watchdog internal oscillator frequency specification. This chapter also describes I/O timing, including programmable I/O element (IOE) delay and programmable output buffer delay.

For more information about the densities and packages of devices in the Cyclone V family, refer to the *Overview for Cyclone V Device Family* chapter.

Electrical Characteristics

The following sections describe the electrical characteristics of Cyclone V devices.

Operating Conditions

Cyclone V devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Cyclone V devices, you must consider the operating requirements described in this chapter.

Cyclone V devices are offered in commercial and industrial grades. Commercial devices are offered in –6 (fastest), –7, and –8 speed grades. Industrial devices are offered in the –7 speed grade.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Cyclone V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

CAUTION

Conditions other than those listed in Table 2–1 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 2–1 lists the Cyclone V absolute maximum ratings.

Table 2–1. Absolute Maximum Ratings for Cyclone V Devices—Preliminary

Symbol	Description	Minimum	Maximum	Unit
V_{CC}	Core voltage and periphery circuitry power supply	TBD	TBD	V
V_{CCPGM}	Configuration pins power supply	TBD	TBD	V
V_{CC_AUX}	Auxiliary supply	TBD	TBD	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	TBD	TBD	V
V_{CCPD}	I/O pre-driver power supply	TBD	TBD	V
V_{CCIO}	I/O power supply	TBD	TBD	V
V_{CCA_FPLL}	PLL analog power supply	TBD	TBD	V
V_{CCH_GXB}	Transceiver high voltage power	TBD	TBD	V
V_{CCE_GXB}	Transceiver power	TBD	TBD	V
V_{CCL_GXB}	Clock network power	TBD	TBD	V
V_I	DC input voltage	TBD	TBD	V
I_{OUT}	DC output current per pin	TBD	TBD	mA
T_J	Operating junction temperature	TBD	TBD	°C
T_{STG}	Storage temperature (No bias)	TBD	TBD	°C

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in Table 2–2 and undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 2–2 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 3.95 V can only be at 3.95 V for ~5% over the lifetime of the device; for a device lifetime of 10 years, this amounts to half a year.

Table 2–2. Maximum Allowed Overshoot During Transitions for Cyclone V Devices—Preliminary

Symbol	Description	Condition (V)	Overshoot Duration as % of High Time	Unit
Vi (AC)	AC input voltage	3.7	100	%
		3.75	59.79	%
		3.8	33.08	%
		3.85	18.45	%
		3.9	10.36	%
		3.95	5.87	%
		4	3.34	%
		4.05	1.92	%
		4.1	1.11	%

Recommended Operating Conditions

Recommended operating conditions are the functional operation limits for the AC and DC parameters for Cyclone V devices.

Table 2–3 lists the steady-state voltage values expected from Cyclone V devices. Power supply ramps must all be strictly monotonic, without plateaus.

Table 2–3. Recommended Operating Conditions for Cyclone V Devices—Preliminary

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CC}	Core voltage, periphery circuitry power supply, transceiver physical coding sublayer (PCS) power supply, and transceiver PCI Express® (PCIe®) hard IP digital power supply	—	1.07	1.1	1.13	V
V_{CC_AUX}	Auxiliary supply	—	2.375	2.5	2.625	V
V_{CCPD}	I/O pre-driver (3.3 V) power supply	—	3.135	3.3	3.465	V
	I/O pre-driver (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O pre-driver (2.5 V) power supply	—	2.375	2.5	2.625	V
V_{CCIO}	I/O buffers (3.3 V) power supply	—	3.135	3.3	3.465	V
	I/O buffers (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O buffers (2.5 V) power supply	—	2.375	2.5	2.625	V
	I/O buffers (1.8 V) power supply	—	1.71	1.8	1.89	V
	I/O buffers (1.5 V) power supply	—	1.425	1.5	1.575	V
	I/O buffers (1.35 V) power supply	—	1.283	1.35	1.418	V
	I/O buffers (1.25 V) power supply	—	1.19	1.25	1.31	V
	I/O buffers (1.2 V) power supply	—	1.14	1.2	1.26	V
V_{CCPGM}	Configuration pins (3.3 V) power supply	—	3.135	3.3	3.465	V
	Configuration pins (3.0 V) power supply	—	2.85	3.0	3.15	V
	Configuration pins (2.5 V) power supply	—	2.375	2.5	2.625	V
	Configuration pins (1.8 V) power supply	—	1.71	1.8	1.89	V
V_{CCA_FPLL} (1)	PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
V_{CCBAT} (2)	Battery back-up power supply (For design security volatile key register)	—	1.2	—	3.0	V
V_I	DC input voltage	—	–0.5	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	Commercial	0	—	85	°C
		Industrial	–40	—	100	°C
t_{RAMP}	Power supply ramp time	Standard POR (PORSEL=0)	200 µs	—	100 ms	—
		Fast POR (PORSEL=1)	200 µs	—	4 ms	—

Notes to Table 2–3:

(1) PLL digital voltage is regulated from V_{CCA_FPLL}.

(2) If you do not use the design security feature in Cyclone V devices, connect V_{CCBAT} to a 1.5-V, 2.5-V, or 3.0-V power supply. The power-on reset (POR) circuitry monitors V_{CCBAT}. Cyclone V devices do not exit POR if V_{CCBAT} stays low.

Table 2–4 lists the transceiver power supply recommended operating conditions for Cyclone V GX devices.

Table 2–4. Transceiver Power Supply Operating Conditions for Cyclone V GX Devices—Preliminary

Symbol	Description	Minimum	Typical	Maximum	Unit
V_{CCH_GXBL}	Transceiver high voltage power (left side)	2.375	2.5	2.625	V
V_{CCE_GXBL}	Transmitter and receiver power (left side)	1.07	1.1	1.13	V
V_{CCL_GXBL}	Clock network power (left side)	1.07	1.1	1.13	V

Table 2–5 lists the steady-state voltage values expected from Cyclone V system-on-a-chip (SoC) FPGA with ARM®-based hard processor system (HPS). Power supply ramps must all be strictly monotonic, without plateaus.

Table 2–5. HPS Power Supply Operating Conditions for Cyclone V SE, SX, and ST Devices—Preliminary

Symbol	Description	Minimum	Typical	Maximum	Unit
V_{CC_HPS}	HPS core voltage and periphery circuitry power supply	1.07	1.1	1.13	V
V_{CCPD_HPS}	HPS I/O pre-driver (3.3 V) power supply	3.135	3.3	3.465	V
	HPS I/O pre-driver (3.0 V) power supply	2.85	3.0	3.15	V
	HPS I/O pre-driver (2.5 V) power supply	2.375	2.5	2.625	V
V_{CCIO_HPS}	HPS I/O buffers (3.3 V) power supply	3.135	3.3	3.465	V
	HPS I/O buffers (3.0 V) power supply	2.85	3.0	3.15	V
	HPS I/O buffers (2.5 V) power supply	2.375	2.5	2.625	V
	HPS I/O buffers (1.8 V) power supply	1.71	1.8	1.89	V
	HPS I/O buffers (1.5 V) power supply	1.425	1.5	1.575	V
	HPS I/O buffers (1.2 V) power supply	1.14	1.2	1.26	V
$V_{CCRSTCLK\_HPS}$	HPS reset and clock input pins (3.3 V) power supply	3.135	3.3	3.465	V
	HPS reset and clock input pins (3.0 V) power supply	2.85	3.0	3.15	V
	HPS reset and clock input pins (2.5 V) power supply	2.375	2.5	2.625	V
	HPS reset and clock input pins (1.8 V) power supply	1.71	1.8	1.89	V
V_{CCPLL_HPS}	HPS PLL analog voltage regulator power supply	2.375	2.5	2.625	V

DC Characteristics

This section lists the supply current, I/O pin leakage current, input pin capacitance, on-chip termination tolerance, and hot socketing specifications.

Supply Current

Standby current is the current drawn from the respective power rails used for power budgeting. Use the Excel-based Early Power Estimator (EPE) to estimate supply current for your design because these currents vary greatly with the resources you use.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

I/O Pin Leakage Current

Table 2–6 lists the Cyclone V I/O pin leakage current specifications.

Table 2–6. I/O Pin Leakage Current for Cyclone V Devices—Preliminary

Symbol	Description	Conditions	Min	Typ	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIOMAX}$	–30	—	30	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0 V to $V_{CCIOMAX}$	–30	—	30	µA

Bus Hold Specifications

Table 2–7 lists the Cyclone V device bus hold specifications.

Table 2–7. Bus Hold Parameters for Cyclone V Devices—Preliminary *(1)*

Parameter	Symbol	Conditions	V_{CCIO} (V)												Unit
			1.2		1.5		1.8		2.5		3.0		3.3		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, sustaining current	I_{SUSL}	$V_{IN} > V_{IL}$ (max.)	8	—	12	—	30	—	50	—	70	—	70	—	µA
Bus-hold, high, sustaining current	I_{SUSH}	$V_{IN} < V_{IH}$ (min.)	–8	—	–12	—	–30	—	–50	—	–70	—	–70	—	µA
Bus-hold, low, overdrive current	I_{ODL}	$0V < V_{IN} < V_{CCIO}$	—	125	—	175	—	200	—	300	—	500	—	500	µA
Bus-hold, high, overdrive current	I_{ODH}	$0V < V_{IN} < V_{CCIO}$	—	–125	—	–175	—	–200	—	–300	—	–500	—	–500	µA
Bus-hold trip point	V_{TRIP}	—	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

Note to Table 2–7:

(1) The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power up for I/O pins connected to the calibration block. Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Table 2–8 lists the Cyclone V OCT termination calibration accuracy specifications.

Table 2–8. OCT Calibration Accuracy Specifications for Cyclone V Devices—Preliminary *(1)*

Symbol	Description	Conditions (V)	Calibration Accuracy			Unit
			C6 Speed Grade	C7, I7 Speed Grade	C8 Speed Grade	
25-Ω R_S	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%
50-Ω R_S	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%
34-Ω and 40-Ω R_S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2	±15	±15	±15	%
48-Ω, 60-Ω, and 80-Ω R_S	Internal series termination with calibration (48-Ω, 60-Ω, and 80-Ω setting)	V_{CCIO} = 1.2	±15	±15	±15	%
50-Ω R_T	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 2.5, 1.8, 1.5, 1.2	-10 to +40	-10 to +40	-10 to +40	%
20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω R_T	Internal parallel termination with calibration (20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25	-10 to +40	-10 to +40	-10 to +40	%
60-Ω and 120-Ω R_T	Internal parallel termination with calibration (60-Ω and 120-Ω setting)	V_{CCIO} = 1.2	-10 to +40	-10 to +40	-10 to +40	%
25-Ω $R_{S\_left\_shift}$	Internal left shift series termination with calibration (25-Ω $R_{S\_left\_shift}$ setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%

Note to Table 2–8:

(1) OCT calibration accuracy is valid at the time of calibration only.

Table 2–9 lists the Cyclone V OCT without calibration resistance tolerance to PVT changes.

Table 2–9. OCT Without Calibration Resistance Tolerance Specifications for Cyclone V Devices—Preliminary

Symbol	Description	Conditions (V)	Resistance Tolerance			Unit
			C6 Speed Grade	C7, I7 Speed Grade	C8 Speed Grade	
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.0 and 2.5	±30	±40	±40	%
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.8 and 1.5	±30	±40	±40	%
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.2	±35	±50	±50	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.0 and 2.5	±30	±40	±40	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8 and 1.5	±30	±40	±40	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.2	±35	±50	±50	%
100-Ω R_D	Internal differential termination (100-Ω setting)	V_{CCIO} = 2.5	±25	TBD	TBD	%

OCT calibration is automatically performed at power up for the OCT-enabled I/O pins. Table 2–10 lists OCT variation with temperature and voltage after power-up calibration. Use Table 2–10 to determine the OCT variation after power-up calibration and Equation 2–1 to determine the OCT variation without recalibration.

Equation 2–1. OCT Variation Without Recalibration—Preliminary *(1), (2), (3), (4), (5), (6)*

$$R_{OCT} = R_{SCAL}\left(1 + \langle\frac{dR}{dT} \times \Delta T\rangle \pm \langle\frac{dR}{dV} \times \Delta V\rangle\right)$$

Notes to Equation 2–1:

(1) The R_{OCT} value calculated from Equation 2–1 shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
(2) R_{SCAL} is the OCT resistance value at power-up.
(3) ΔT is the variation of temperature with respect to the temperature at power up.
(4) ΔV is the variation of voltage with respect to V_{CCIO} at power up.
(5) dR/dT is the percentage change of R_{SCAL} with temperature.
(6) dR/dV is the percentage change of R_{SCAL} with voltage.

Table 2–10 lists the OCT variation after the power-up calibration.

Table 2–10. OCT Variation after Power-Up Calibration for Cyclone V Devices—Preliminary (1)

Symbol	Description	V_{CCIO} (V)	Typical	Unit
dR/dV	OCT variation with voltage without recalibration	3.0	0.0297	%/mV
		2.5	0.0344	
		1.8	0.0499	
		1.5	0.0744	
		1.2	0.1241	
dR/dT	OCT variation with temperature without recalibration	3.0	0.189	%/°C
		2.5	0.208	
		1.8	0.266	
		1.5	0.273	
		1.2	0.317	

Note to Table 2–10:

(1) Valid for a V_{CCIO} range of ±5% and a temperature range of 0° to 85°C.

Pin Capacitance

Table 2–11 lists the Cyclone V device family pin capacitance.

Table 2–11. Pin Capacitance for Cyclone V Devices

Symbol	Description	Value	Unit
C_{IOTB}	Input capacitance on top and bottom I/O pins	5.5	pF
C_{IOLR}	Input capacitance on left and right I/O pins	5.5	pF
C_{OUTFB}	Input capacitance on dual-purpose clock output and feedback pins	5.5	pF

Hot Socketing

Table 2–12 lists the hot socketing specifications for Cyclone V devices.

Table 2–12. Hot Socketing Specifications for Cyclone V Devices—Preliminary

Symbol	Description	Maximum
$I_{IOPIN\ (DC)}$	DC current per I/O pin	300 µA
$I_{IOPIN\ (AC)}$	AC current per I/O pin	8 mA (1)
$I_{XCVR\text{-}TX\ (DC)}$	DC current per transceiver transmitter (TX) pin	100 mA
$I_{XCVR\text{-}RX\ (DC)}$	DC current per transceiver receiver (RX) pin	50 mA

Note to Table 2–12:

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C\ dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.

Internal Weak Pull-Up Resistor

Table 2–13 lists the weak pull-up resistor values for Cyclone V devices.

Table 2–13. Internal Weak Pull-Up Resistor Values for Cyclone V Devices—Preliminary *(1), (2)*

Symbol	Description	Conditions (V) *(3)*	Typ *(4)*	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you have enabled the programmable pull-up resistor option.	V_{CCIO} = 3.3 ±5%	25	kΩ
		V_{CCIO} = 3.0 ±5%	25	kΩ
		V_{CCIO} = 2.5 ±5%	25	kΩ
		V_{CCIO} = 1.8 ±5%	25	kΩ
		V_{CCIO} = 1.5 ±5%	25	kΩ
		V_{CCIO} = 1.35 ±5%	25	kΩ
		V_{CCIO} = 1.25 ±5%	25	kΩ
		V_{CCIO} = 1.2 ±5%	25	kΩ

Notes to Table 2–13:

(1) All I/O pins have an option to enable weak pull-up except the configuration, test, and JTAG pins.

(2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ.

(3) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

(4) These specifications are valid with ±10% tolerances to cover changes over PVT.

I/O Standard Specifications

Table 2–14 through Table 2–19 list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Cyclone V devices. These tables also list the Cyclone V device family I/O standard specifications. The V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL}, respectively.

For an explanation of terms used in Table 2–14 through Table 2–19, refer to "Glossary" on page 2–35.

Table 2–14. Single-Ended I/O Standards for Cyclone V Devices—Preliminary (Part 1 of 2)

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3-V LVTTL	3.135	3.3	3.465	–0.3	0.8	1.7	3.6	0.45	2.4	4	–4
3.3-V LVCMOS	3.135	3.3	3.465	–0.3	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	2	–2
3.0-V LVTTL	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.4	2.4	2	–2
3.0-V LVCMOS	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	0.1	–0.1
3.0-V PCI	2.85	3	3.15	—	0.3 x V_{CCIO}	0.5 x V_{CCIO}	V_{CCIO} + 0.3	0.1 x V_{CCIO}	0.9 x V_{CCIO}	1.5	–0.5
3.0-V PCI-X	2.85	3	3.15	—	0.35 x V_{CCIO}	0.5 x V_{CCIO}	V_{CCIO} + 0.3	0.1 x V_{CCIO}	0.9 x V_{CCIO}	1.5	–0.5
2.5 V	2.375	2.5	2.625	–0.3	0.7	1.7	3.6	0.4	2	1	–1
1.8 V	1.71	1.8	1.89	–0.3	0.35 x V_{CCIO}	0.65 x V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} – 0.45	2	–2

Table 2–14. Single-Ended I/O Standards for Cyclone V Devices—Preliminary (Part 2 of 2)

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
1.5 V	1.425	1.5	1.575	–0.3	0.35 x V_{CCIO}	0.65 x V_{CCIO}	V_{CCIO} + 0.3	0.25 x V_{CCIO}	0.75 x V_{CCIO}	2	–2
1.2 V	1.14	1.2	1.26	–0.3	0.35 x V_{CCIO}	0.65 x V_{CCIO}	V_{CCIO} + 0.3	0.25 x V_{CCIO}	0.75 x V_{CCIO}	2	–2

Table 2–15. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications for Cyclone V Devices—Preliminary

I/O Standard	V_{CCIO}(V)			V_{REF}(V)			V_{TT}(V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}
SSTL 135 Class I, II	1.283	1.35	1.418	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}
SSTL 125 Class I, II	1.19	1.25	1.26	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	V_{CCIO}/2	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	V_{CCIO}/2	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 x V_{CCIO}	0.5 x V_{CCIO}	0.53 x V_{CCIO}	—	V_{CCIO}/2	—
HSUL-12	1.14	1.2	1.3	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}	—	—	—

Table 2–16. Single-Ended SSTL and HSTL I/O Standards Signal Specifications for Cyclone V Devices—Preliminary (Part 1 of 2)

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{ol} (mA)	I_{oh} (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-2 Class I	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} – 0.31	V_{REF} + 0.31	V_{TT} – 0.608	V_{TT} + 0.608	8.1	–8.1
SSTL-2 Class II	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} – 0.31	V_{REF} + 0.31	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
SSTL-18 Class I	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	V_{TT} – 0.603	V_{TT} + 0.603	6.7	–6.7
SSTL-18 Class II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	0.28	V_{CCIO} – 0.28	13.4	–13.4
SSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 x V_{CCIO}	0.8 x V_{CCIO}	8	–8
SSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 x V_{CCIO}	0.8 x V_{CCIO}	16	–16
SSTL 135	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.16	V_{REF} + 0.16	TBD (1)	TBD (1)	TBD (1)	TBD (1)

Table 2–16. Single-Ended SSTL and HSTL I/O Standards Signal Specifications for Cyclone V Devices—Preliminary (Part 2 of 2)

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{ol} (mA)	I_{oh} (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL 125	—	V_{REF} – 0.85	V_{REF} + 0.85	—	V_{REF} – 0.15	V_{REF} + 0.15	TBD (1)	TBD (1)	TBD (1)	TBD (1)
HSTL-18 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 x V_{CCIO}	0.75 x V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 x V_{CCIO}	0.75 x V_{CCIO}	16	–16
HSUL-12	—	V_{REF} – 0.13	V_{REF} + 0.13	—	V_{REF} – 0.22	V_{REF} + 0.22	0.1 x V_{CCIO}	0.9 x V_{CCIO}	TBD (1)	TBD (1)

Note to Table 2–16:

(1) Pending silicon characterization.

Table 2–17. Differential SSTL I/O Standards for Cyclone V Devices—Preliminary

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)		$V_{OX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V_{CCIO} + 0.6	V_{CCIO}/2 – 0.2	—	V_{CCIO}/2 + 0.2	0.62	V_{CCIO} + 0.6	V_{CCIO}/2 – 0.15	—	V_{CCIO}/2 + 0.15
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V_{CCIO} + 0.6	V_{CCIO}/2 – 0.175	—	V_{CCIO}/2 + 0.175	0.5	V_{CCIO} + 0.6	V_{CCIO}/2 – 0.125	—	V_{CCIO}/2 + 0.125
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	–0.2	-0.15	—	0.15	–0.35	0.35	—	V_{CCIO}/2	—
SSTL 135	1.283	1.35	1.45	0.2	–0.2	V_{REF} – 0.135	V_{CCIO}/2	V_{REF} + 0.135	TBD (1)	TBD (1)	V_{REF} – 0.15	—	V_{REF} + 0.15
SSTL 125	1.19	1.25	1.31	TBD (1)	—	TBD (1)	V_{CCIO}/2	TBD (1)	TBD (1)	—	TBD (1)	TBD (1)	TBD (1)

Note to Table 2–17:

(1) Pending silicon characterization.

Table 2–18. Differential HSTL I/O Standards for Cyclone V Devices—Preliminary

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V_{CCIO} + 0.3	—	0.5 x V_{CCIO}	—	0.4 x V_{CCIO}	0.5 x V_{CCIO}	0.6 x V_{CCIO}	0.3	V_{CCIO} + 0.48
HSUL-12	1.14	1.2	1.3	0.26	0.26	0.5 x V_{CCIO} – 0.12	0.5 x V_{CCIO}	0.5 x V_{CCIO} +0.12	0.4 x V_{CCIO}	0.5 x V_{CCIO}	0.6 x V_{CCIO}	0.44	0.44

Table 2–19. Differential I/O Standard Specifications for Cyclone V Devices—Preliminary *(1)*

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)			$V_{ICM(DC)}$ (V)		V_{OD} (V) *(2)*			V_{OCM} (V) *(2)*		
	Min	Typ	Max	Min	Condition	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
PCML	Transmitter, receiver, and input reference clock pins of high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to Table 2–20 on page 2–13.													
2.5 V LVDS	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	1.8	0.247	—	0.6	1.125	1.25	1.375
RSDS (HIO)	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.3	1.4	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (HIO)	2.375	2.5	2.625	200	—	600	0.4	1.325	0.25	—	0.6	1	1.2	1.4
LVPECL	2.375	2.5	2.625	300	—	—	0.6	1.8	—	—	—	—	—	—

Notes to Table 2–19:

(1) The 1.4-V and 1.5-V PCML transceiver I/O standard specifications are described in "Transceiver Performance Specifications" on page 2–13.

(2) RL range: 90 ≤ RL ≤ 110 Ω

Power Consumption

Altera offers two ways to estimate power consumption for a design—the Excel-based Early Power Estimator (EPE) and the Quartus® II PowerPlay Power Analyzer feature.

You typically use the interactive Excel-based EPE before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

Switching Characteristics

This section provides performance characteristics of Cyclone V core and periphery blocks for commercial grade devices.

These characteristics can be designated as preliminary or final.

- Preliminary characteristics are obtained using simulation results, process data, and other known parameters. The title of these tables show the designation as "Preliminary."
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

Transceiver Performance Specifications

This section describes transceiver performance specifications.

Table 2–20 lists the Cyclone V GX transceiver specifications.

Table 2–20. Transceiver Specifications for Cyclone V GX Devices—Preliminary (Part 1 of 3)

Symbol/ Description	Conditions	C6 Speed Grade			C7, I7 Speed Grade			C8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Clock											
Supported I/O Standards	**1.2 V PCML, 1.5 V PCML, 2.5 V PCML, Differential LVPECL** (1), **HCSL**, and **LVDS**										
Input frequency from REFCLK input pins	—	27	—	550	27	—	550	27	—	550	MHz
Duty cycle	—	45	—	55	45	—	55	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	2000	200	—	2000	200	—	2000	mV
Spread-spectrum modulating clock frequency	PCIe	30	—	33	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5%	—	—	0 to –0.5%	—	—	0 to –0.5%	—	—
On-chip termination resistors	—	—	100	—	—	100	—	—	100	—	Ω
V_{ICM} (AC coupled)	—	1.1 (2)			1.1 (2)			1.1 (2)			V
V_{ICM} (DC coupled)	**HCSL** I/O standard for the PCIe reference clock	250	—	550	250	—	550	250	—	550	mV
R_{REF}	—	—	2000 ±1%	—	—	2000 ±1%	—	—	2000 ±1%	—	Ω

Table 2–20. Transceiver Specifications for Cyclone V GX Devices—Preliminary (Part 2 of 3)

Symbol/ Description	Conditions	C6 Speed Grade			C7, I7 Speed Grade			C8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Transceiver Clocks											
`fixedclk` clock frequency	PCIe Receiver Detect	—	125	—	—	125	—	—	125	—	MHz
Avalon® Memory-Mapped (Avalon-MM) PHY management clock frequency	< 150										MHz
Receiver											
Supported I/O Standards	**1.5 V PCML, 2.5 V PCML, LVPECL**, and **LVDS**										
Data rate	—	614	—	3125	614	—	3125	614	—	2500	Mbps
Absolute V_{MAX} for a receiver pin *(3)*	—	—	—	1.2	—	—	1.2	—	—	1.2	V
Absolute V_{MIN} for a receiver pin	—	–0.4	—	—	–0.4	—	—	–0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration	—	—	—	2.2	—	—	2.2	—	—	2.2	V
Minimum differential eye opening at the receiver serial input pins *(4)*	—	85	—	—	85	—	—	85	—	—	mV
Differential on-chip termination resistors	85–Ω setting	—	85	—	—	85	—	—	85	—	Ω
	100–Ω setting	—	100	—	—	100	—	—	100	—	Ω
	120–Ω setting	—	120	—	—	120	—	—	120	—	Ω
	150-Ω setting	—	150	—	—	150	—	—	150	—	Ω
Differential and common mode return loss	PCIe Gen1, GIGE	Compliant									—
Programmable PPM detector *(5)*	—	±62.5, 100, 125, 200, 250, 300, 500, and 1000									ppm
Run Length	—	—	—	200	—	—	200	—	—	200	UI
Programmable equalization	—	—	—	4	—	—	4	—	—	4	dB
Programmable DC gain	DC Gain Setting = 0	—	0	—	—	0	—	—	0	—	dB
	DC Gain Setting = 1	—	3	—	—	3	—	—	3	—	dB

Table 2–20. Transceiver Specifications for Cyclone V GX Devices—Preliminary (Part 3 of 3)

Symbol/ Description	Conditions	C6 Speed Grade			C7, I7 Speed Grade			C8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Transmitter											
Supported I/O Standards	**1.5 V PCML**										
Data rate	—	614	—	3125	614	—	3125	614	—	2500	Mbps
V_{OCM}	—	—	650	—	—	650	—	—	650	—	mV
Differential on-chip termination resistors	85–Ω setting	—	85	—	—	85	—	—	85	—	Ω
	100–Ω setting	—	100	—	—	100	—	—	100	—	Ω
	120–Ω setting	—	120	—	—	120	—	—	120	—	Ω
	150-Ω setting	—	150	—	—	150	—	—	150	—	Ω
Rise time *(6)*	—	30	—	160	30	—	160	30	—	160	ps
Fall time *(6)*	—	30	—	160	30	—	160	30	—	160	ps
CMU PLL											
Supported data range	—	614	—	3125	614	—	3125	614	—	2500	Mbps
Transceiver-FPGA Fabric Interface											
Interface speed (single-width mode)	—	25	—	187.5	25	—	163.84	25	—	156.25	MHz
Interface speed (double-width mode)	—	25	—	163.84	25	—	163.84	25	—	156.25	MHz

Notes to Table 2–20:

(1) Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.

(2) The reference clock common mode voltage is equal to the V_{CCR_GXB} power supply level.

(3) The device cannot tolerate prolonged operation at this absolute maximum.

(4) The differential eye opening specification at the receiver input pins assumes that you have disabled the Receiver Equalization feature. If you enable the Receiver Equalization feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(5) The rate matcher supports only up to ±300 parts per million (ppm).

(6) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.

Table 2–21 lists the Cyclone V GX transceiver block jitter specifications.

Table 2–21. Transceiver Block Jitter Specifications for Cyclone V GX Devices—Preliminary

Symbol/ Description	Conditions	C6 Speed Grade			C7, I7 Speed Grade			C8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
PCIe Transmit Jitter Generation (1)											
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern	—	—	0.25	—	—	0.25	—	—	0.25	UI
PCIe Receiver Jitter Tolerance (1)											
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern	> 0.6			> 0.6			> 0.6			UI
GIGE Transmit Jitter Generation (2)											
Deterministic jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.14	—	—	0.14	—	—	0.14	UI
Total jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.279	—	—	0.279	—	—	0.279	UI
GIGE Receiver Jitter Tolerance (2)											
Deterministic jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.4			> 0.4			> 0.4			UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.66			> 0.66			> 0.66			UI

Notes to Table 2–21:

(1) The jitter numbers for PIPE are compliant to the PCIe Base Specification 2.0.

(2) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.

Core Performance Specifications

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), and memory block specifications.

Clock Tree Specifications

Table 2–22 lists the clock tree specifications for Cyclone V devices.

Table 2–22. Clock Tree Performance for Cyclone V Devices—Preliminary

Symbol	Performance			Unit
	C6 Speed Grade	C7, I7 Speed Grade	C8 Speed Grade	
Global clock and Regional clock	550	550	460	MHz
Peripheral clock	155	155	155	MHz

PLL Specifications

Table 2–23 lists the Cyclone V PLL specifications when operating in both the commercial junction temperature range (0° to 85°C) and the industrial junction temperature range (–40° to 100°C).

Table 2–23. PLL Specifications for Cyclone V Devices—Preliminary (1) (Part 1 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input clock frequency (–6 speed grade)	5	—	670 (2)	MHz
	Input clock frequency (–7 speed grade)	5	—	622 (2)	MHz
	Input clock frequency (–8 speed grade)	5	—	500 (2)	MHz
f_{INPFD}	Integer input clock frequency to the PFD	5	—	325	MHz
f_{FINPFD}	Fractional input clock frequency to the PFD	50	—	TBD (1)	MHz
f_{VCO}	PLL VCO operating range (–6 speed grade)	600	—	1600	MHz
	PLL VCO operating range (–7 speed grade)	600	—	1400	MHz
	PLL VCO operating range (–8 speed grade)	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	40	—	60	%
f_{OUT}	Output frequency for internal global or regional clock (–6 speed grade)	—	—	550 (3)	MHz
	Output frequency for internal global or regional clock (–7 speed grade)	—	—	550 (3)	MHz
	Output frequency for internal global or regional clock (–8 speed grade)	—	—	460 (3)	MHz
f_{OUT_EXT}	Output frequency for external clock output (–6 speed grade)	—	—	667 (3)	MHz
	Output frequency for external clock output (–7 speed grade)	—	—	667 (3)	MHz
	Output frequency for external clock output (–8 speed grade)	—	—	533 (3)	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	50	55	%
t_{FCOMP}	External feedback clock compensation time	—	—	10	ns

Table 2–23. PLL Specifications for Cyclone V Devices—Preliminary (1) (Part 2 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{CONFIGPHASE}$	Time required to reconfigure phase shift	—	—	TBD (1)	—
$t_{DYCONFIGCLK}$	Dynamic configuration clock	—	—	100	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of areset	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	1	ms
f_{CLBW}	PLL closed-loop low bandwidth	—	0.3	—	MHz
	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth (8)	—	4	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the areset signal	10	—	—	ns
t_{INCCJ} (4), (5)	Input clock cycle-to-cycle jitter ($F_{REF} \geq 100$ MHz)	—	—	0.15	UI (p-p)
	Input clock cycle-to-cycle jitter ($F_{REF} < 100$ MHz)	—	—	±750	ps (p-p)
t_{OUTPJ_DC} (6)	Period jitter for dedicated clock output ($F_{OUT} \geq 100$ MHz)	—	—	TBD (1)	ps (p-p)
	Period jitter for dedicated clock output ($F_{OUT} < 100$ MHz)	—	—	TBD (1)	mUI (p-p)
t_{OUTCCJ_DC} (6)	Cycle-to-cycle jitter for dedicated clock output ($F_{OUT} \geq 100$ MHz)	—	—	TBD (1)	ps (p-p)
	Cycle-to-cycle jitter for dedicated clock output ($F_{OUT} < 100$ MHz)	—	—	TBD (1)	mUI (p-p)
t_{OUTPJ_IO} (6), (9)	Period jitter for clock output on regular I/O ($F_{OUT} \geq 100$ MHz)	—	—	TBD (1)	ps (p-p)
	Period jitter for clock output on regular I/O ($F_{OUT} < 100$ MHz)	—	—	TBD (1)	mUI (p-p)
t_{OUTCCJ_IO} (6), (9)	Cycle-to-cycle jitter for clock output on regular I/O ($F_{OUT} \geq 100$ MHz)	—	—	TBD (1)	ps (p-p)
	Cycle-to-cycle jitter for clock output on regular I/O ($F_{OUT} < 100$ MHz)	—	—	TBD (1)	mUI (p-p)
$t_{OUTPJ\_DC\_F}$	Period jitter for dedicated clock output in fractional mode	—	—	TBD (1)	—
$t_{OUTCCJ\_DC\_F}$	Cycle-to-cycle jitter for dedicated clock output in fractional mode	—	—	TBD (1)	—
$t_{OUTPJ\_IO\_F}$	Period jitter for clock output on regular I/O in fractional mode	—	—	TBD (1)	—
$t_{OUTCCJ\_IO\_F}$	Cycle-to-cycle jitter for clock output on regular I/O in fractional mode	—	—	TBD (1)	—
$t_{CASC\_OUTPJ\_DC}$ (6), (7)	Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} \geq 100$ MHz)	—	—	TBD (1)	ps (p-p)
	Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} < 100$ MHz)	—	—	TBD (1)	mUI (p-p)
t_{DRIFT}	Frequency drift after PFDENA is disabled for a duration of 100 µs	—	—	±10	%
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	—	24	—	Bits
k_{VALUE}	Numerator of Fraction	TBD (1)	8388608	TBD (1)	—

Table 2–23. PLL Specifications for Cyclone V Devices—Preliminary (1) (Part 3 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
f_{RES}	Resolution of VCO frequency (f_{INPFD} =100 MHz)	—	5.96	—	Hz

Notes to Table 2–23:

(1) Pending silicon characterization.

(2) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(3) This specification is limited by the lower of the two: I/O f_{MAX} or F_{OUT} of the PLL.

(4) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source < 120 ps.

(5) F_{REF} is $f_{IN/N}$ when N = 1.

(6) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 2–28 on page 2–23.

(7) The cascaded PLL specification is only applicable with the following condition:
a. Upstream PLL: 0.59 MHz ≤ Upstream PLL BW < 1 MHz
b. Downstream PLL: Downstream PLL BW > 2 MHz

(8) High bandwidth PLL settings are not supported in external feedback mode.

(9) External memory interface clock output jitter specifications use a different measurement method, which is available in Table 2–28 on page 2–23.

DSP Block Specifications

Table 2–24 lists the Cyclone V DSP block performance specifications.

Table 2–24. DSP Block Performance Specifications for Cyclone V Devices—Preliminary

Mode	Performance			Unit
	C6 Speed Grade	C7, I7 Speed Grade	C8 Speed Grade	
Modes using One DSP Block				
Independent 9 x 9 Multiplication	340	300	260	MHz
Independent 18 x 19 Multiplication	287	250	200	MHz
Independent 18 x 18 Multiplication	287	250	200	MHz
Independent 27 x 27 Multiplication	250	200	160	MHz
Independent 18 x 25 Multiplication	310	250	200	MHz
Independent 20 x 24 Multiplication	310	250	200	MHz
Two 18 x 19 Multiplier Adder Mode	310	250	200	MHz
18 x 18 Multiplier Added Summed with 36-bit Input	310	250	200	MHz
Modes using Two DSP Blocks				
Complex 18 x 19 multiplication	310	250	200	MHz
Two 27 x 27 Multiplier Adder	250	200	160	MHz
Four 18 x 19 Multiplier Adder	310	250	200	MHz

Memory Block Specifications

Table 2–25 lists the Cyclone V memory block specifications.

Table 2–25. Memory Block Performance Specifications for Cyclone V Devices—Preliminary *(1), (2)*

Memory	Mode	Resources Used		Performance			Unit
		ALUTs	Memory	C6 Speed Grade	C7, I7 Speed Grade	C8 Speed Grade	
MLAB	Single port, all supported widths	0	1	450	380	330	MHz
	Simple dual-port, all supported widths	0	1	450	380	330	MHz
	Simple dual-port with read and write at the same address	0	1	350	300	250	MHz
	ROM, all supported width	0	1	450	380	330	MHz
M10K Block	Single-port, all supported widths	0	1	315	275	240	MHz
	Simple dual-port, all supported widths	0	1	315	275	240	MHz
	Simple dual-port with the **read-during-write** option set to **Old Data**, all supported widths	0	1	275	240	180	MHz
	True dual port, all supported widths	0	1	315	275	240	MHz
	ROM, all supported widths	0	1	315	275	240	MHz
	Min Pulse Width (clock high time)	—	—	1,450	1,550	1,650	ps
	Min Pulse Width (clock low time)	—	—	1,000	1,200	1,350	ps

Notes to Table 2–25:

(1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50%** output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

(2) When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in f_{MAX}.

Periphery Performance

This section describes periphery performance and the high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the LVDS high-speed I/O interface, external memory interface, and the PCI/PCI-X bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-V **LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2 **LVCMOS** at 100 MHz interfacing frequency with 10 pF load.

Actual achievable frequency depends on design- and system-specific factors. You must perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

Table 2–26 lists high-speed I/O timing for Cyclone V devices.

Table 2–26. High-Speed I/O Specifications for Cyclone V Devices—Preliminary (2), (3) (Part 1 of 2)

Symbol	Conditions	C6 Speed Grade			C7, I7 Speed Grade			C8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_in} (input clock frequency) True Differential I/O Standards	Clock boost factor W = 1 to 40 (4)	5	—	437.5	5	—	420	5	—	320	MHz
f_{HSCLK_in} (input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40 (4)	5	—	TBD (1)	5	—	TBD (1)	5	—	TBD (1)	MHz
f_{HSCLK_OUT} (output clock frequency)	—	5	—	420	5	—	370	5	—	320	MHz
Transmitter											
True Differential I/O Standards - f_{HSDR} (data rate)	SERDES factor J = 4 to 10	(5)	—	840	(5)	—	740	(5)	—	640	Mbps
	SERDES factor J = 1 to 2, Uses DDR Registers	(5)	—	(7)	(5)	—	(7)	(5)	—	(7)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - f_{HSDR} (data rate) (6)	SERDES factor J = 4 to 10	(5)	—	TBD (1)	(5)	—	TBD (1)	(5)	—	TBD (1)	Mbps
$t_{x\ Jitter}$ - True Differential I/O Standards	Total Jitter for Data Rate, 600 Mbps - 840 Mbps	—	—	160	—	—	160	—	—	160	ps
	Total Jitter for Data Rate, < 600 Mbps	—	—	0.1	—	—	0.1	—	—	0.1	UI
$t_{x\ Jitter}$ - Emulated Differential I/O Standards with Three External Output Resistor Network	Total Jitter for Data Rate, 600 Mbps to maximum data rate supported	—	—	TBD (1)	—	—	TBD (1)	—	—	TBD (1)	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	TBD (1)	—	—	TBD (1)	—	—	TBD (1)	UI
t_{DUTY}	TX output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	45	50	55	%
t_{RISE} & t_{FALL}	True Differential I/O Standards	—	—	200	—	—	200	—	—	200	ps
	Emulated Differential I/O Standards with Three External Output Resistor Networks	—	—	250	—	—	250	—	—	300	ps

Table 2–26. High-Speed I/O Specifications for Cyclone V Devices—Preliminary (2), (3) (Part 2 of 2)

Symbol	Conditions	C6 Speed Grade			C7, I7 Speed Grade			C8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TCCS	True Differential I/O Standards	—	—	200	—	—	250	—	—	250	ps
	Emulated Differential I/O Standards	—	—	300	—	—	300	—	—	300	ps
Receiver											
f_{HSDR} (data rate)	SERDES factor J = 4 to 10	(5)	—	875 (6)	(5)	—	840 (6)	(5)	—	640 (6)	Mbps
	SERDES factor J = 1 to 2, Uses DDR Registers	(5)	—	(7)	(5)	—	(7)	(5)	—	(7)	Mbps
Sampling Window	—	—	—	350	—	—	350	—	—	350	ps

Notes to Table 2–26:

(1) Pending silicon characterization.

(2) When J = 1 or 2, bypass the serializer/deserializer (SERDES) block.

(3) This is achieved by using the LVDS clock network.

(4) Clock Boost Factor (W) is the ratio between the input data rate and the input clock rate.

(5) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

(6) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.

(7) The maximum ideal frequency is the SERDES factor (J) x PLL max output frequency (fout), provided you can close the design timing and the signal integrity simulation is clean.You can estimate the achievable maximum data rate by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

DQS Logic Block and Memory Output Clock Jitter Specifications

Table 2–27 lists the DQS phase shift error for Cyclone V devices.

Table 2–27. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Cyclone V Devices—Preliminary (1), (2)

Number of DQS Delay Buffers	C6 Speed Grade	C7, I7 Speed Grade	C8 Speed Grade	Unit
2	69	70	80	ps

Notes to Table 2–27:

(1) The numbers are preliminary pending silicon characterization.

(2) This error specification is the absolute maximum and minimum error. For example, skew on two DQS delay buffers in a –7 speed grade is 70 ps or ±35 ps.

(3) Delay chain engineering option setting: rb_co[1:0]="11".

Table 2–28 lists the memory output clock jitter specifications for Cyclone V devices.

Table 2–28. Memory Output Clock Jitter Specification for Cyclone V Devices—Preliminary *(1), (2), (3)*

Parameter	Clock Network	Symbol	C6 Speed Grade		C7, I7 Speed Grade		C8 Speed Grade		Unit
			Min	Max	Min	Max	Min	Max	
Clock period jitter	Regional	$t_{JIT(per)}$	TBD	TBD	TBD	TBD	TBD	TBD	ps
Cycle-to-cycle period jitter	Regional	$t_{JIT(cc)}$	TBD	TBD	TBD	TBD	TBD	TBD	ps
Duty cycle jitter	Regional	$t_{JIT(duty)}$	TBD	TBD	TBD	TBD	TBD	TBD	ps
Clock period jitter	Global	$t_{JIT(per)}$	TBD	TBD	TBD	TBD	TBD	TBD	ps
Cycle-to-cycle period jitter	Global	$t_{JIT(cc)}$	TBD	TBD	TBD	TBD	TBD	TBD	ps
Duty cycle jitter	Global	$t_{JIT(duty)}$	TBD	TBD	TBD	TBD	TBD	TBD	ps

Notes to Table 2–28:

(1) Pending silicon characterization.

(2) The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard.

(3) The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.

OCT Calibration Block Specifications

Table 2–29 lists the OCT calibration block specifications for Cyclone V devices.

Table 2–29. OCT Calibration Block Specifications for Cyclone V Devices—Preliminary

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for R_S OCT /R_T OCT calibration	—	1000	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for OCT code to shift out	—	32	—	Cycles
T_{RS_RT}	Time required between the `dyn_term_ctrl` and `oe` signal transitions in a bidirectional I/O buffer to dynamically switch between R_S OCT and R_T OCT	—	2.5	—	ns

Duty Cycle Distortion (DCD) Specifications

Table 2–30 lists the worst-case DCD for Cyclone V devices.

Table 2–30. Worst-Case DCD on I/O Pins for Cyclone V Devices—Preliminary

Symbol	C6 Speed Grade		C7, I7 Speed Grade		C8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	%

Configuration Specification

This section provides configuration specifications and timing for Cyclone V devices.

These characteristics can be designated as preliminary or final.

- Preliminary characteristics are obtained using simulation results, process data, and other known parameters. The title of these tables show the designation as "Preliminary."
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

POR Specifications

Table 2–31 lists the specifications for fast and standard POR delay for Cyclone V devices.

Table 2–31. Fast and Standard POR Delay Specification for Cyclone V Devices

POR Delay	PORSEL Pin Setting	Minimum (ms)	Maximum (ms)
Fast (1)	High	4	12
Standard	GND	100	300

Note to Table 2–31:

(1) The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the PCIe hard IP to initialize after the POR trip.

JTAG Configuration Timing

Table 2–32 lists the JTAG timing parameters and values for Cyclone V devices.

Table 2–32. JTAG Timing Parameters and Values for Cyclone V Devices—Preliminary

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period	30	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU\ (TDI)}$	TDI JTAG port setup time	1	—	ns
$t_{JPSU\ (TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	11 (1)	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14 (1)	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14 (1)	ns

Note to Table 2–32:

(1) A 1 ns adder is required for each V_{CCIO} voltage step down from 3.0 V. For example, t_{JPCO} = 12 ns if V_{CCIO} of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

FPP Configuration Timing

This section describes the fast passive parallel (FPP) configuration timing parameters for Cyclone V devices.

DCLK-to-DATA[] Ratio (r) for FPP Configuration

FPP configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

Table 2–33 lists the DCLK-to-DATA[] ratio for each combination.

Table 2–33. DCLK-to-DATA[] Ratio for Cyclone V Devices—Preliminary *(1)*

Configuration Scheme	Encryption	Compression	DCLK-to-DATA[] ratio (r)
FPP (8-bit wide)	Off	Off	1
	On	Off	1
	Off	On	2
	On	On	2
FPP (16-bit wide)	Off	Off	1
	On	Off	2
	Off	On	4
	On	On	4

Note to Table 2–33:

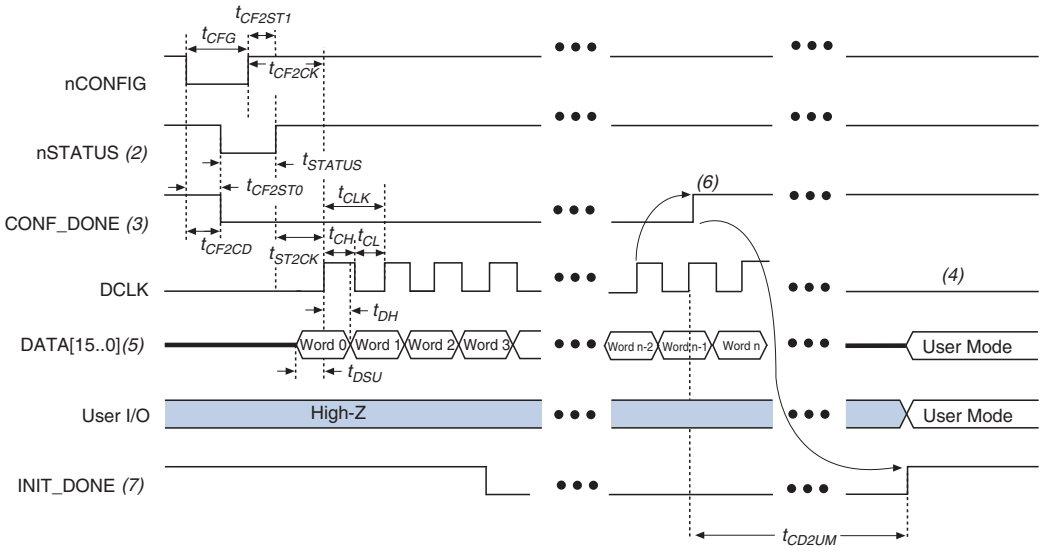
(1) Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is r times the DATA[] rate in byte per second (Bps) or word per second (Wps). For example, in FPP x16 where the r is 2, the DCLK frequency must be 2 times the DATA[] rate in Wps.

FPP Configuration Timing when DCLK to DATA[] = 1

Figure 2–1 shows the timing waveform for an FPP configuration when using a MAX® II device as an external host. This waveform shows timing when the DCLK-to-DATA[] ratio is 1.

When you enable decompression or the design security feature, the DCLK-to-DATA[] ratio varies for FPP x8 and FPP x16. For the respective DCLK-to-DATA[] ratio, refer to Table 2–33 on page 2–25.

Figure 2–1. DCLK-to-DATA[] FPP Configuration Timing Waveform for Cyclone V Devices When the Ratio is 1 (1)



Notes to Figure 2–1:

(1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.

(2) After power up, the Cyclone V device holds nSTATUS low for the time of the POR delay.

(3) After power up, before and during configuration, CONF_DONE is low.

(4) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.

(5) For FPP x16, use DATA[15..0]. For FPP x8, use DATA[7..0]. DATA[15..0] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.

(6) To ensure a successful configuration, send the entire configuration data to the Cyclone V device. CONF_DONE is released high when the Cyclone V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.

(7) After the option bit to enable the INIT_DONE pin is configured into the device, INIT_DONE goes low.

Table 2–34 lists the timing parameters for Cyclone V devices for an FPP configuration when the DCLK-to-DATA[] ratio is 1.

Table 2–34. DCLK-to-DATA[] FPP Timing Parameters for Cyclone V Devices When the Ratio is 1—Preliminary *(1)*

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1506 *(2)*	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1506 *(3)*	µs
t_{CF2CK}	nCONFIG high to first rising edge on DCLK	1506	—	µs
t_{ST2CK}	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	0.45 x $1/f_{MAX}$	—	ns
t_{CL}	DCLK low time	0.45 x $1/f_{MAX}$	—	ns
t_{CLK}	DCLK period	$1/f_{MAX}$	—	ns
f_{MAX}	DCLK frequency (FPP x8 and x16)	—	125	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode *(4)*	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} x CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	17,408	—	Cycles

Notes to Table 2–34:

(1) Use these timing parameters when the DCLK-to-DATA[] ratio is 1. To find the DCLK-to-DATA[] ratio for your system, refer to Table 2–33 on page 2–25.

(2) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

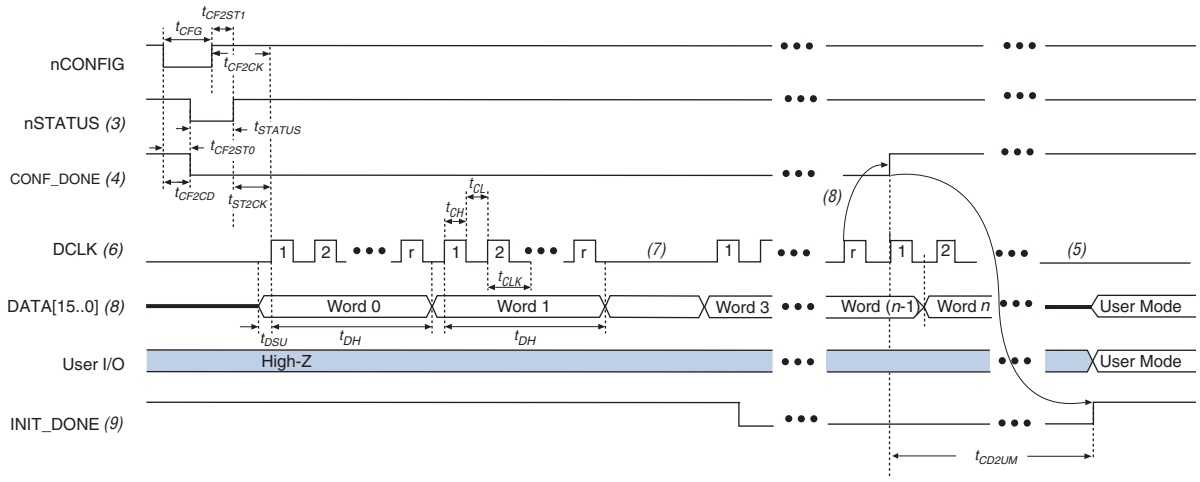
(3) You can obtain this value if you do not delay configuration by externally holding nSTATUS low.

(4) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

FPP Configuration Timing when DCLK to DATA[] > 1

Figure 2–2 shows the timing waveform for an FPP configuration when using a MAX II device or microprocessor as an external host. This waveform shows timing when the DCLK-to-DATA[] ratio is more than 1.

Figure 2–2. FPP Configuration Timing Waveform for Cyclone V Devices When the DCLK-to-DATA[] Ratio is > 1 *(1), (2)*



Notes to Figure 2–2:

(1) To find the DCLK-to-DATA[] ratio for your system, refer to Table 2–33 on page 2–25.

(2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.

(3) After power up, the Cyclone V device holds nSTATUS low for the time as specified by the POR delay.

(4) After power up, before and during configuration, CONF_DONE is low.

(5) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.

(6) "r" denotes the DCLK-to-DATA[] ratio. For the DCLK-to-DATA[] ratio based on the decompression and the design security feature enable settings, refer to Table 2–33 on page 2–25.

(7) If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA[15..0] pins prior to sending the first DCLK rising edge.

(8) To ensure a successful configuration, send the entire configuration data to the Cyclone V device. CONF_DONE is released high after the Cyclone V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.

(9) After the option bit to enable the INIT_DONE pin is configured into the device, INIT_DONE goes low.

Table 2–35 lists the timing parameters for Cyclone V devices when the DCLK-to-DATA[] ratio is more than 1.

Table 2–35. DCLK-to-DATA[] FPP Timing Parameters for Cyclone V Devices when the Ratio is > 1—Preliminary *(1)*

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1506 *(2)*	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1506 *(3)*	µs
t_{CF2CK}	nCONFIG high to first rising edge on DCLK	1506	—	µs
t_{ST2CK}	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	3 x $1/f_{DCLK}$	—	ns
t_{CH}	DCLK high time	0.45 x $1/f_{MAX}$	—	ns
t_{CL}	DCLK low time	0.45 x $1/f_{MAX}$	—	ns
t_{CLK}	DCLK period	$1/f_{MAX}$	—	ns
f_{MAX}	DCLK frequency (FPP x8 and x16)	—	125	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode *(4)*	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} x CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	17,408	—	Cycles

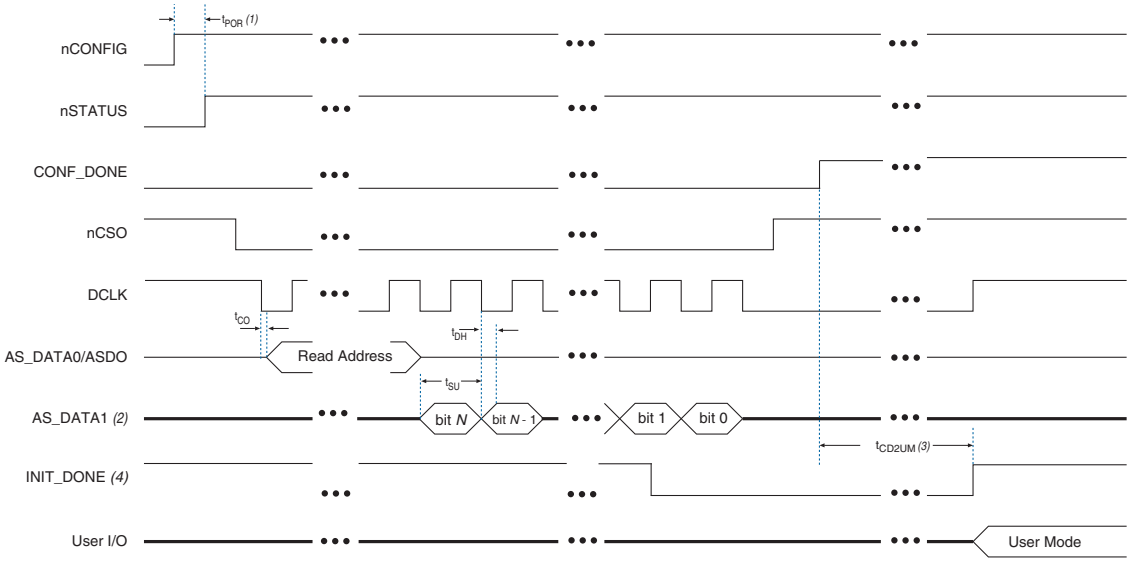
Notes to Table 2–35:

(1) Use these timing parameters when you use decompression and the design security features.
(2) This value can be obtained if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
(3) This value can be obtained if you do not delay configuration by externally holding nSTATUS low.
(4) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

AS Configuration Timing

Figure 2–3 shows the timing waveform for the active serial (AS) x1 mode and AS x4 mode configuration timing.

Figure 2–3. AS Configuration Timing for Cyclone V Devices



Notes to Figure 2–3:

(1) The AS scheme supports standard and fast POR delay (t_{POR}). For t_{POR} delay information, refer to "POR Delay Specification" in the *Configuration, Design Security, and remote System Upgrades in Cyclone V Devices* chapter.

(2) If you are using AS x4 mode, this signal represents the AS_DATA[3..0] and EPCQ sends in 4-bits of data for each DCLK cycle.

(3) The initialization clock can be from the internal oscillator or the CLKUSR pin.

(4) After the option bit to enable the INIT_DONE pin is configured into the device, INIT_DONE goes low.

Table 2–36 lists the timing parameters for AS x1 and AS x4 configurations in Cyclone V devices.

Table 2–36. AS Timing Parameters for AS x1 and x4 Configurations in Cyclone V Devices—Preliminary (1), (2)

Symbol	Parameter	Minimum	Maximum	Unit
t_{CO}	DCLK falling edge to the AS_DATA0/ASDO output	—	4	µs
t_{SU}	Data setup time before the rising edge on DCLK	1.5	—	ns
t_H	Data hold time after the rising edge on DCLK	0	—	ns
t_{CD2UM}	CONF_DONE high to user mode	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 x maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} x CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	17,408	—	Cycles

Notes to Table 2–36:

(1) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

(2) The t_{CF2CD}, t_{CF2ST0}, t_{CFG}, t_{STATUS}, and t_{CF2ST1} timing parameters are identical to the timing parameters for passive serial (PS) mode listed in Table 2–38 on page 2–32.

Table 2–37 lists the internal clock frequency specification for the AS configuration scheme.

Table 2–37. DCLK Frequency Specification in the AS Configuration Scheme for Cyclone V Devices—Preliminary *(1), (2)*

Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz
10.6	15.7	25.0	MHz
21.3	31.4	50.0	MHz
42.6	62.9	100.0	MHz

Notes to Table 2–37:

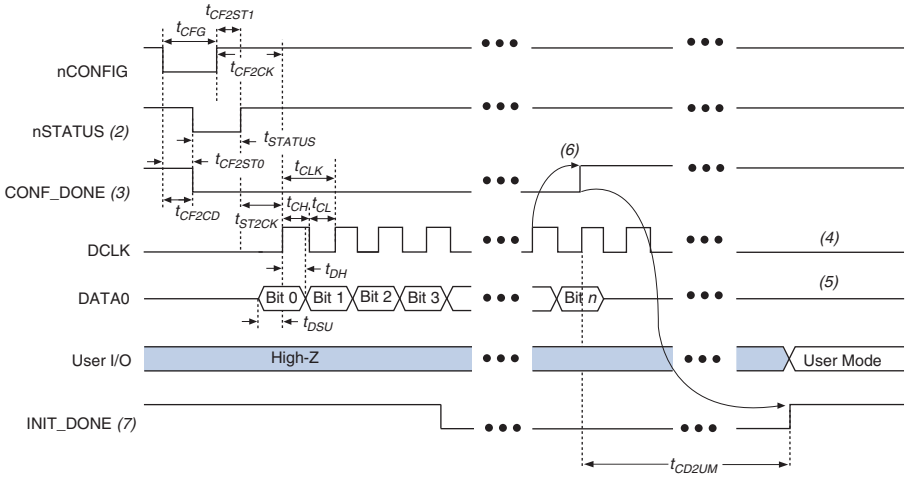
(1) This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.

(2) The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

PS Configuration Timing

Figure 2–4 shows the timing waveform for a PS configuration when using a MAX II device or microprocessor as an external host.

Figure 2–4. PS Configuration Timing Waveform for Cyclone V Devices *(1)*



Notes to Figure 2–4:

(1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.

(2) After power up, the Cyclone V device holds nSTATUS low for the time of the POR delay.

(3) After power up, before and during configuration, CONF_DONE is low.

(4) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.

(5) DATA0 is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the **Device and Pins Option**.

(6) To ensure a successful configuration, send the entire configuration data to the Cyclone V device. CONF_DONE is released high after the Cyclone V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.

(7) After the option bit to enable the INIT_DONE pin is configured into the device, INIT_DONE goes low.

Table 2–38 lists the PS timing parameter for Cyclone V devices.

Table 2–38. PS Timing Parameters for Cyclone V Devices—Preliminary

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1506 (1)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1506 (2)	µs
t_{CF2CK}	nCONFIG high to first rising edge on DCLK	1506	—	µs
t_{ST2CK}	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	0.45 x $1/f_{MAX}$	—	ns
t_{CL}	DCLK low time	0.45 x $1/f_{MAX}$	—	ns
t_{CLK}	DCLK period	$1/f_{MAX}$	—	ns
f_{MAX}	DCLK frequency	—	125	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode (3)	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 x maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} x CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	17,408	—	Cycles

Notes to Table 2–38:

(1) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(2) You can obtain this value if you do not delay configuration by externally holding nSTATUS low.

(3) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

Remote System Upgrades Circuitry Timing Specification

Table 2–39 lists the timing parameter specifications for the remote system upgrade circuitry.

Table 2–39. Remote System Upgrade Circuitry Timing Specification for Cyclone V Devices—Preliminary

Parameter	Minimum	Maximum	Unit
$t_{MAX\_RU\_CLK}$ (1)	—	40	MHz
$t_{RU\_nCONFIG}$ (2)	250	—	ns
$t_{RU\_nRSTIMER}$ (3)	250	—	ns

Notes to Table 2–39:

(1) This clock is user-supplied to the remote system upgrade circuitry. If you are using the ALTREMOTE_UPDATE megafunction, the clock user-supplied to the ALTREMOTE_UPDATE megafunction must meet this specification.

(2) This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE megafunction high for the minimum timing specification. For more information, refer to "Remote System Upgrade State Machine" in the *Device Interfaces and Integration Basics for Cyclone V Devices* chapter.

(3) This is equivalent to strobing the reset timer input of the ALTREMOTE_UPDATE megafunction high for the minimum timing specification. For more information, refer to "User Watchdog Timer" in the *Device Interfaces and Integration Basics for Cyclone V Devices* chapter.

User Watchdog Internal Oscillator Frequency Specification

Table 2–40 lists the frequency specifications for the user watchdog internal oscillator.

Table 2–40. User Watchdog Internal Oscillator Frequency Specifications for Cyclone V Devices—Preliminary

Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz

I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

The Excel-based I/O Timing spreadsheet will be available in the future release of the Quartus II software.

Programmable IOE Delay

Table 2–41 lists the Cyclone V IOE programmable delay settings.

Table 2–41. IOE Programmable Delay for Cyclone V Devices *(1)*

Parameter	Available Settings	Minimum Offset	Fast Model		Slow Model			Unit
			Industrial	Commercial	C6 Speed Grade	C7, I7 Speed Grade	C8 Speed Grade	
TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns

Note to Table 2–41:

(1) Pending data extraction from the Quartus II software.

Programmable Output Buffer Delay

Table 2–42 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

Table 2–42. Programmable Output Buffer Delay for Cyclone V Devices—Preliminary *(1), (2)*

Symbol	Parameter	Typical	Unit
D_{OUTBUF}	Rising and/or falling edge delay	0 (default)	ps
		50	ps
		100	ps
		150	ps

Notes to Table 2–42:

(1) Pending data extraction from the Quartus II software.

(2) You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

Glossary

Table 2–43 lists the glossary for this chapter.

Table 2–43. Glossary Table (Part 1 of 4)

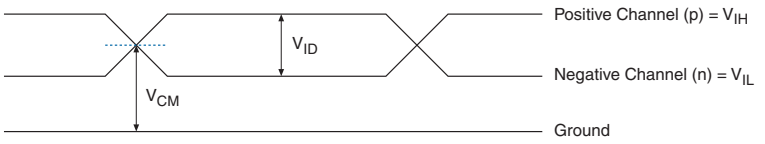
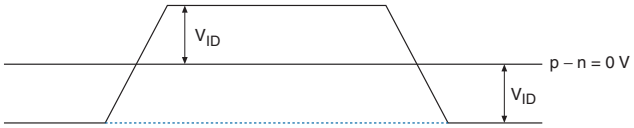
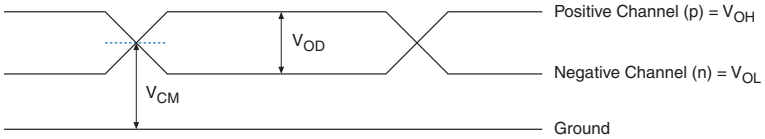
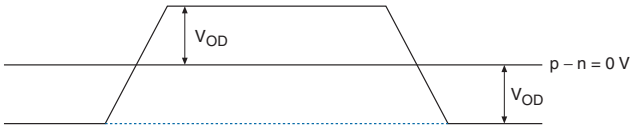
Letter	Subject	Definitions
A B C	—	—
D	Differential I/O Standards	*Receiver Input Waveforms* **Single-Ended Waveform**  **Differential Waveform**  *Transmitter Output Waveforms* **Single-Ended Waveform**  **Differential Waveform** 
E	—	—
F	f_{HSCLK}	Left/right PLL input clock frequency.
	f_{HSDR}	High-speed I/O block—Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
	$f_{HSDRDPA}$	High-speed I/O block—Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
G H I	—	—

Table 2–43. Glossary Table (Part 2 of 4)

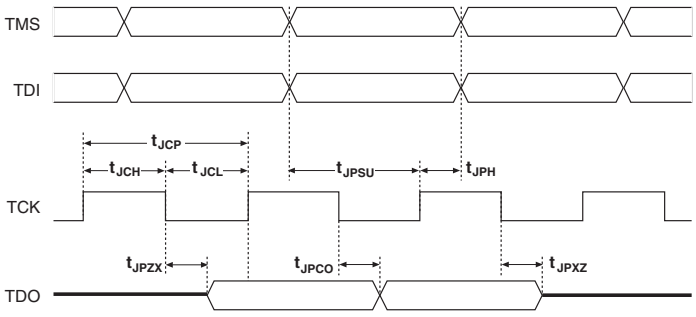
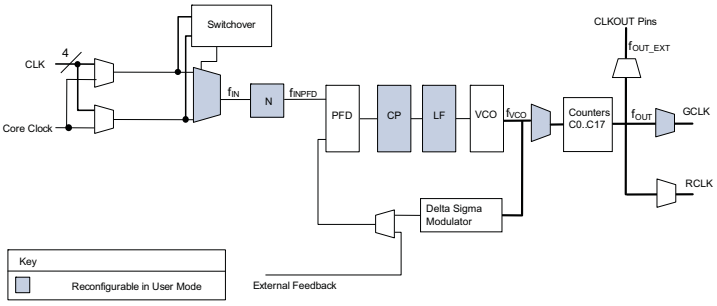
Letter	Subject	Definitions
J	J	High-speed I/O block—Deserialization factor (width of parallel data bus).
J	JTAG Timing Specifications	JTAG Timing Specifications: 
K L M N O	—	—
P	PLL Specifications	**Diagram of PLL Specifications** *(1)*  **Note:** (1) `Core Clock` can only be fed by dedicated clock input pins or PLL outputs.
Q	—	—
R	R_L	Receiver differential input discrete resistor (external to the Cyclone V device).

Table 2–43. Glossary Table (Part 3 of 4)

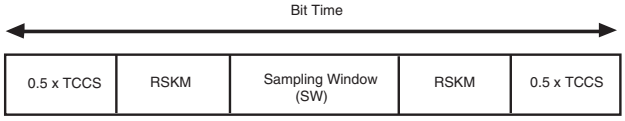
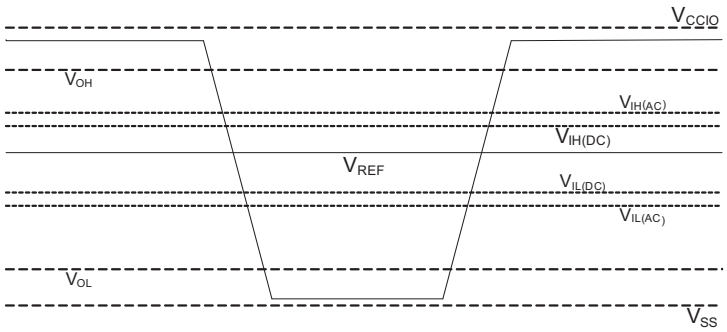
Letter	Subject	Definitions
S	Sampling window (SW)	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown: 
	Single-ended voltage referenced I/O standard	The JEDEC standard for the **SSTI** and **HSTL** I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the AC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing, as shown: *Single-Ended Voltage Referenced I/O Standard* 
T	t_C	High-speed receiver/transmitter input and output clock period.
	TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including the t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the *Timing Diagram* figure under **SW** in this table).
	t_{DUTY}	High-speed I/O block—Duty cycle on high-speed transmitter output clock. **Timing Unit Interval (TUI)** The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w)
	t_{FALL}	Signal high-to-low transition time (80-20%)
	t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input
	t_{OUTPJ_IO}	Period jitter on the general purpose I/O driven by a PLL
	t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL
	t_{RISE}	Signal low-to-high transition time (20–80%)
U	—	—

Table 2–43. Glossary Table (Part 4 of 4)

Letter	Subject	Definitions
V	$V_{CM(DC)}$	DC common mode input voltage.
	V_{ICM}	Input common mode voltage—The common mode of the differential signal at the receiver.
	V_{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	$V_{DIF(AC)}$	AC differential input voltage—Minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential input voltage— Minimum DC input differential voltage required for switching.
	V_{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage
	$V_{IH(DC)}$	High-level DC input voltage
	V_{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
	$V_{IL(AC)}$	Low-level AC input voltage
	$V_{IL(DC)}$	Low-level DC input voltage
	V_{OCM}	Output common mode voltage—The common mode of the differential signal at the transmitter.
	V_{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
	V_{SWING}	Differential input voltage
	V_X	Input differential cross point voltage
	V_{OX}	Output differential cross point voltage
W	W	High-speed I/O block—Clock Boost Factor
X Y Z	—	—

Document Revision History

Table 2–44 lists the revision history for this chapter.

Table 2–44. Document Revision History

Date	Version	Changes
November 2011	1.1	■ Added Table 2–5. ■ Updated Table 2–3, Table 2–4, Table 2–11, Table 2–13, Table 2–20, and Table 2–21.
October 2011	1.0	Initial release.

This chapter provides additional information about the document and Altera.

How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

Contact (1)	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Nontechnical support (general)	Email	nacomp@altera.com
(software licensing)	Email	authorization@altera.com

Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, **Save As** dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, **\qdesigns** directory, **D:** drive, and **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Indicate document titles. For example, *Stratix IV Design Guidelines*.
italic type	Indicates variables. For example, *n* + 1. Variable names are enclosed in angle brackets (< >). For example, *<file name>* and *<project name>***.pof** file.
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.
"Subheading Title"	Quotation marks indicate references to sections in a document and titles of Quartus II Help topics. For example, "Typographic Conventions."

Visual Cue	Meaning
`Courier type`	Indicates signal, port, register, bit, block, and primitive names. For example, `data1`, `tdi`, and `input`. The suffix `n` denotes an active-low signal. For example, `resetn`. Indicates command line commands and anything that must be typed exactly as it appears. For example, `c:\qdesigns\tutorial\chiptrip.gdf`. Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword `SUBDESIGN`), and logic function names (for example, `TRI`).
↵	An angled arrow instructs you to press the Enter key.
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■ ■	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
	The question mark directs you to a software help system with related information.
	The feet direct you to another document or website with related information.
	The multimedia icon directs you to a related multimedia presentation.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
	A warning calls attention to a condition or possible situation that can cause you injury.
	The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.